A Wireless Multi-Channel Peripheral Nerve Signal Acquisition System-on-Chip

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***Abstract*— The adoption of chronic implantable peripheral nerve-based prosthetic devices is currently hampered by the lack of a highly integrated neural signal acquisition system-on-chip (SoC). We report a ten-channel peripheral nervous system (PNS) electroneurogram (ENG) signal acquisition SoC within an implantable package. Requiring only four off-chip capacitors, this SoC can be co-encapsulated with flexible nerve electrodes and a resonant coil antenna to form a 3.4 cm^3 and 3.9 g implantable device for chronic ENG acquisition. This SoC is inductively powered and controlled through a resonant coil at 22 MHz and transmits the digitized neural signal through a near-infrared LED (NIR-LED). Fabricated in 0.18-μm CMOS, each amplifier channel exhibits an input referred noise of 1.9 μV_{rms} and a noise efficiency factor (NEF) of 4.0 within the signal bandwidth of 5.5 kHz. Each amplifier channel within the SoC is digitized with 10-bit resolution at 17.5 ksps, and the total power consumption (SoC and NIR-LED) is 4.4 mW when the NIR-LED is driven at 3 Mb/s. An electrode impedance measurement circuit with <10% magnitude and <8° angle error for measuring impedances up to 1 MΩ is also incorporated in this SoC. This wireless, low noise ENG acquisition SoC package has been validated *in vivo* while implanted on a rodent to acquire ENG from its sciatic nerve.**

***Index Terms*— Amplifier, CMOS, common-mode feedback (CMFB), common-mode rejection ratio (CMRR), input common-mode range, low power, low voltage, low-noise amplifier, neural prosthesis, neural recording amplifier, peripheral nerve, peripheral nerve signal, signal acquisition.**

I. Introduction

PERIPHERAL nerve prostheses (PNP) [1], [2] and electronic medicine (EM) [3], [4] are options that complement surgical approaches to restore control of paralyzed limbs and pharmaceutical therapies to restore physiological homeostasis, respectively. Both approaches require the recording of weak electroneurogram (ENG) signals from peripheral nerves, following which the acquired signals are used either to assess the efficacy of EM or to activate downstream prosthetic devices. To date, many promising applications of peripheral nerve ENG acquisition, such as that in [1] and [2], have been demonstrated. However, they remain limited to percutaneous electrical interfaces tethered to benchtop instrumentation. Such setups pose higher risks of transdermal infection, are not portable, and are prone to electrode failure due to cable breakage, and therefore cannot be translated into a full standalone implantable PNP/EM system.

To achieve a practical, fully implantable peripheral nerve ENG acquisition device, the recorded neural signal data needs to be transmitted to external post-processing devices via an untethered and transcutaneous interfacing method. Additional challenging electrical and biomechanical requirements need to be addressed at the same time. Similar to miniaturized cortical acquisition systems [5], [6], the electrical requirements include the need to dissipate the lowest power possible, while being self-powered and to contain low input-referred noise levels. Low power consumption allows for a longer self-powered device run time and reduces heat loss, thereby minimizing potential damage to the surrounding tissue. Action potentials acquired in cortical regions can be as high as 1.2 mV_{pp} [7], while peripheral nerve ENG signals acquired using intraneural electrodes comprise voltage amplitudes only as high as 400 μV_{pp} [8]. Therefore, peripheral nerve ENG

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amplifiers recording from intraneural electrodes require lower input-referred noise levels than that of neural amplifiers for cortical signal acquisition. Furthermore, unlike the cortical acquisition setups that are mounted on the skull, peripheral nerve ENG acquisition devices must be implanted in soft tissue, and would hence require a compact form factor and compliant surfaces. Hermetic encapsulation using biocompatible and flexible materials is also required to ensure long-term device reliability.

Several peripheral nerve ENG acquisition systems have been reported [9], [10]. These devices utilize inductive power coupling for transcutaneous powering and data telemetry. However, these proof-of-concept devices still have a relatively large form factor due to the use of large or multiple off-the-shelf components. A smaller device was reported in [11], but it required a two-chip implementation and a long (>5 cm) external monopole antenna for data telemetry.

To overcome the abovementioned limitations, an implantable peripheral nerve ENG acquisition device using a single system-on-chip (SoC) with minimal off-chip components incorporated is preferred. The functions of wireless power recovery, ENG signal recording, digitization, and data telemetry would be incorporated in such an SoC. Although several SoCs for the central nervous system (CNS) have some of these functions [12]–[14], they either do not achieve sufficient noise level performance for peripheral nerve ENG acquisition or do not contain wireless data and power transfer on a single chip.

In this paper, we report the first peripheral nerve ENG acquisition SoC that meets the requirements defined earlier. A peripheral nerve ENG acquisition device only requires this single chip SoC to compactly integrate nerve electrodes, near-field power harvesting, and data telemetry. This SoC has potential clinical applications in which desired recording sites for decoding movement intent are located separately from targeted stimulation sites, e.g., recording from proximal nerves while performing functional electrical stimulation of hand muscles in paralyzed patients [15].

This paper is organized as follows. The SoC architecture is introduced in Section II, and its circuit-level implementations for key sub-blocks are described in Section III. The supporting external reader unit for this SoC is described in Section IV. Electrical and *in vivo* measurements are reported in Section V.

II. System Overview and Design Considerations

This peripheral nerve ENG acquisition SoC has been designed with the goal of creating a compact device integrated with flexible intraneural electrode interfaces such as the thin-film longitudinal intrafascicular electrode (tf-LIFE). While the previous work in [16] focuses only on multichannel recording amplifiers, this work focuses on the integration of several functions on a single chip. These functions include neural signal amplification, analog-to-digital conversion, wireless power and command recovery, on-chip power and clock delivery, data telemetry, and electrode impedance measurement to meet the system specifications and minimize off-chip passive components. The multi-channel neural amplifier circuit in this work adopts the same topology as that in [16], but has been redesigned in a 0.18-μm CMOS process technology and

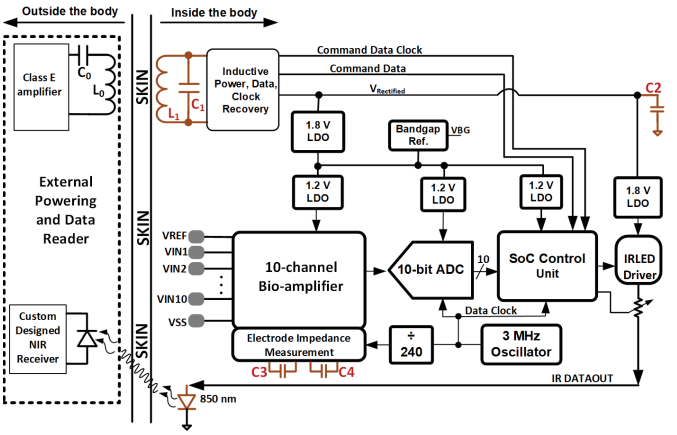

Fig. 1. System block diagram of proposed SoC. Besides the inductive coil (L_1) and 850-nm NIR-LED, only four off-chip capacitors (C_1–C_4) are required for full SoC functionality.

optimized for low input referred noise required for peripheral nerve ENG acquisition. Aside from an inductive coil for receiving inductive power, only four surface-mount (SMD) ceramic capacitors are required for full SoC functionality. The system level block diagram is illustrated in Fig. 1.

The first system level consideration during the design of the SoC was the choice of output data telemetry. Implantable acquisition devices either use two-coil near-field proximity coupling [17], [18] or far-field radio frequency (RF) data transmission [11], [19]. The two-coil solution removes the need for a high frequency power carrier to support high-speed load shift keying (LSK) data telemetry on a single coil. Instead, the first coil powers the device while the second coil is energized at a much higher frequency than that of the power coil, allowing output data telemetry rates of up to 2 Mb/s for a 20-MHz data carrier frequency [17]. Further increase of the data rate would lead to a more elaborate design of the carrier generator to operate at higher frequencies since the fractional bandwidth is limited by the minimum quality factor needed for communication at a specific range. Having two separate coils also increases the form factor of the devices. Furthermore, based on our experience in [18], the two-coil implementation is susceptible to inter-coil coupling which affects data and power reception and demands a minimum physical separation distance between both coils.

Output data telemetry using RF transmission, such as the 402–405-MHz frequency band [19], [20], has also been used for implantable devices. Nonetheless, they are confined to data rates of less than 800 kb/s and require antenna sizes comparable to the coils for LSK data telemetry. A 433-MHz system was reported in [11] with 9 Mb/s output data telemetry. However, its one-way ON-OFF keying RF link lacks a handshake protocol; therefore external electromagnetic interference would potentially affect data reception.

In this paper, we prioritized the need to obtain high-speed data reliably transmitted across the skin to an external unit with a small implant form factor. The received data can then be transferred for downstream post-processing using either wired protocols, such as the universal serial bus (USB) or wireless protocols such as the IEEE 802.11 (WIFI). We observed

that NIR data transmission has already been demonstrated for transcutaneous data telemetry at rates of up to 80 Mb/s over 3-mm skin thickness with low bit-error rates (BER) of 10^{-14} [21]. NIR data telemetry was also successfully demonstrated at 13.56 Mb/s in a cortical implant system for a nonhuman primate [22]. In both studies, only a single NIR emitter was required for the implant device. Such emitters are now commonly available as near-infrared LEDs (NIR-LEDs), with high-power efficiencies at sizes of less than 5 mm^2 which is much smaller than the previously mentioned implementations. The characteristics of transcutaneous NIR transmission have also been reported in [23]. In view of the small form factor and proven reliable data communication, we chose NIR data transmission for our high-speed transcutaneous output data telemetry. The NIR data transmission can simultaneously operate with the inductive powering on the same external receiver.

For low-noise ENG acquisition, it is crucial to incorporate a low-noise power supply for the neural amplifier system and the ADC even when the SoC is inductively powered. In this paper, this is achieved by first decoupling the rectified voltage with the use of an off-chip 10-nF capacitor, C_2, while driving a two-layered network of on-chip capacitor-less low-dropout regulators (CL-LDO). Each of the CL-LDOs would not require any off-chip capacitors to maintain loop stability. Each CL-LDO only requires 300 pF of decoupling capacitance to maintain good transient load responses. Such capacitance can be easily achieved with arrays of MOSFET capacitors that occupy unused space on the chip. The first 1.8-V CL-LDO drives dedicated 1.2-V CL-LDOs for the neural amplifier, ADC and the SoC control unit (SCU). Measurement results in Section V revealed that the neural amplifiers experienced only $<10\ mV_{pp}$ of supply noise when the SoC was inductively powered. A separate 1.8-V CL-LDO powers the NIR-LED driver, thereby minimizing the reverse coupling of the NIR-LED switching noise to the rest of the supply rails.

To perform low-noise ENG acquisition, a ten-channel peripheral nerve ENG amplifier is included on-chip and its outputs are time multiplexed to drive an on-chip 10-bit ADC. The on-chip ADC is a low power, symmetrical switching SAR ADC that was previously described in [24].

Users of neural acquisition devices need to determine the integrity of each recording electrode through electrode impedance measurements. Very high or very low electrode impedances are telltale signs of a faulty electrode and could account for non-physiological signals acquired on the corresponding channels. An electrode impedance measurement circuit (EIM) is hence included on-chip to measure impedance across any selected channel and the reference input (VREF), with its output digitized by the same on-chip ADC. The EIM circuit also shares the same 1.2-V supply rail as the neural amplifiers.

To provide a stable clock for the on-chip ADC, SCU, and EIM circuit, a 3-MHz relaxation oscillator is integrated on-chip. Having this on-chip oscillator also gives the SoC added flexibility to be powered inductively at different carrier frequencies without affecting the output data throughput. This oscillator is digitally tunable over a 5-bit range to counter the effect of process variations on the oscillation frequency.

Clock and command data from an external reader are recovered on-chip to program the SCU. The SCU provides control signals to the various on-chip circuits to orchestrate the digitization and transmission of multi-channel digitized neural data (or electrode impedance measurements) in the universal asynchronous receive/transmit (UART) format. Through the SCU, the number of transmitted amplifier channels could be scaled from 1 to 10. When all 10 channels are acquired, the effective sample rate per channel is 17.85 ks/s.

III. VLSI Circuit Design

Sections III-A–III-D describe the individual circuit blocks illustrated in Fig. 1 in further detail.

A. Ten-Channel PNS Neural Amplifier

Very low noise peripheral nerve ENG amplifiers were previously reported in [25] and [26], and were designed to acquire very low amplitude signals ($<10\ \mu V_{pp}$) [27] from extraneural electrodes. These devices feature an input referred noise level of $<300\ nV_{rms}$ across a noise bandwidth of 5 [26] and 10 kHz [25], respectively. However, each of these amplifiers consumed more than 1 mW to achieve a very low thermal noise floor and required bipolar transistors (which are not compatible with mainstream CMOS processes) at their inputs to obtain low $1/f$ noise. Although the $1/f$ noise component can be easily removed by chopper stabilization, a high chopper frequency is required for neural signal bandwidths of up to 5 kHz, and the amplifier power consumption would correspondingly be increased.

In this paper, the neural amplifier is designed for recording ENGs from tf-LIFE electrodes. These electrodes can be secured in close proximity to the nerve fibers which result in much higher signal amplitudes being recorded compared to extraneural electrodes as described earlier. The use of tf-LIFE electrodes relieves the low noise requirement and power consumption of the neural amplifier. In addition, most recorded peripheral nerve ENG signal frequency content is located below 6 kHz [1], [28], hence the neural amplifier can be band limited to reduce the total in-band thermal noise contribution. The total input referred noise is targeted at less than 3 μV_{rms} for a signal bandwidth of 6 kHz.

Fig. 2 shows the schematic of the ten-channel neural amplifier in this work. The neural amplifier was previously reported in [16] but has been redesigned in this work in a 0.18-μm CMOS process and with reduced input referred noise for peripheral nervous system (PNS) ENG acquisition. A single-ended, capacitively coupled LNA (CCLNA) functions as the front-end amplifier, and is based on the CMOS-inverter-based OTA (CI_OTA) reported in [16]. The CI_OTA has the advantage of having most of its supply current dedicated to maximizing the combined transconductance (g_m) of M_{P1} and M_{N1}. For a total bias current of 13 μA, a low thermal noise floor of 10 $nV/\sqrt{Hz}$ was achieved when simulated in Cadence Spectre. M_{P1} and M_{N1} are also optimally sized to minimize the $1/f$ noise component [29]. To achieve high open-loop gain with a sufficient output swing while being powered at 0.65 V

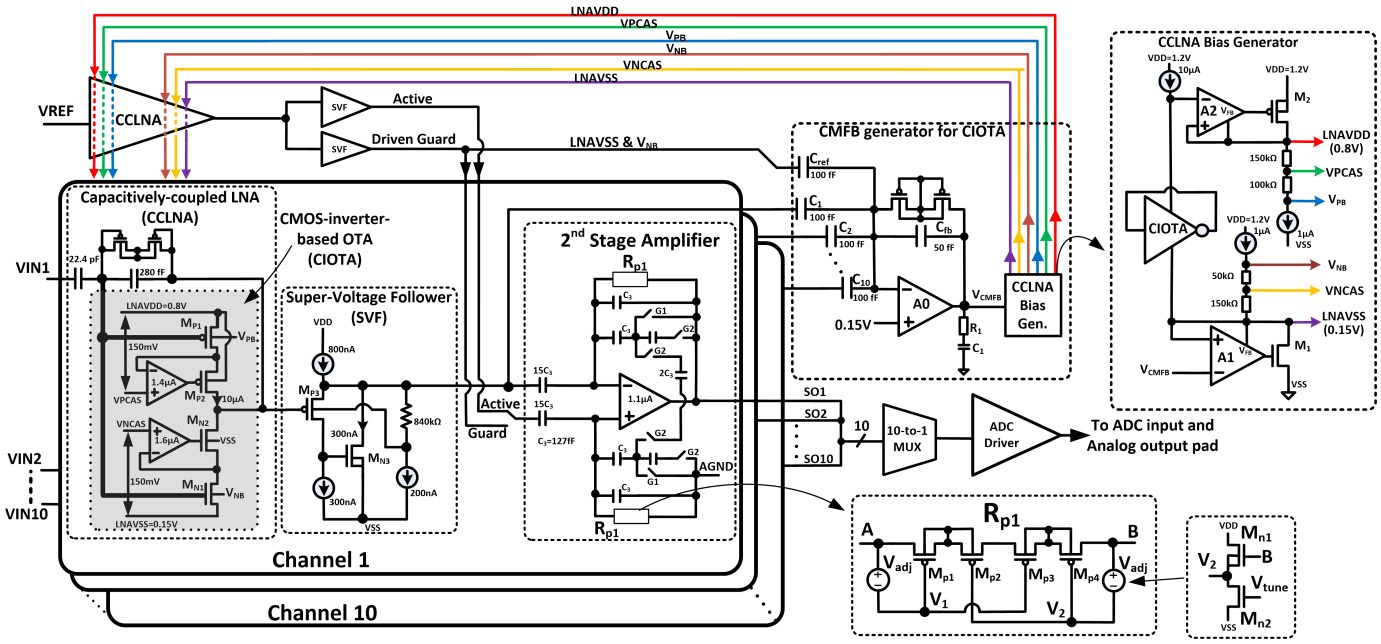

Fig. 2. Circuit block diagram of the ten-Channel PNS neural amplifier. Circuit topologies for OTA A0–A2 are similar to that described in [16]. Lower-right inset also shows the circuit schematic of the proposed cross-coupled complimentary pseudo-resistor (Rp1) and its source follower that is represented in the voltage source, V_{adj}.

and under 10 μA bias current through M_{P1} and M_{N1}, the regulated cascode topology is employed. The common-mode feedback (CMFB) technique described in the next paragraph supplies the 0.65 V for the CI_OTA.

A replica amplifier topology is employed for the ten-channel neural amplifier comprising ten CCLNAs and an additional CCLNA as the reference channel. In the presence of common-mode interference such as stray electromyogram (EMG) signals from surrounding muscles or from the ac mains, the front-end amplifiers in a conventional replica amplifier topology can be easily saturated. Therefore, a CMFB through the supply rails (LNAVDD and LNAVSS) first proposed in [16] is employed for the multi-channel replica amplifiers. The circuit for generating the CMFB through the supply rails is shown in Fig. 2 (right). Similar to the technique described in [16], a 10-μA current flows through the master CI_OTA to effectively generate a fixed dc potential of 0.65 V between LNAVDD and LNAVSS. Compared to [16], the CI_OTA in this work required regulated cascodes to enable high gain operation at 0.65V. Therefore, the CMFB generator included additional voltage generators (VPCAS and VNCAS) for setting the drain-source voltages of M_{P1} and M_{N1}. This replica amplifier topology has two other advantages compared to the conventional neural amplifier [30], [31]. First, the impedances of the reference and signal inputs are the same, providing high total CMRR (TCMRR) [16]. Second, only a single input capacitor, and hence less area, is required per channel compared to two input capacitors required in conventional neural recording amplifiers. The additional 100-fF capacitor per channel (C_{ref}, $C_1 \ldots C_{10}$ in Fig. 2) for the CMFB circuit is much smaller than that of the input capacitor (22.4 pF). Therefore, they do not contribute significantly to the amplifier area per channel as compared to the input capacitor.

For reliable operation at 1.2 V over simulated process and temperature corners, the super source follower (SSF) [32] rather than the flipped voltage follower of [16] is used as the pre-driver to the second amplifier stage inputs. Forward bulk bias is incorporated to increase the transconductance of M_{P3}, which increases the bandwidth and decreases the output impedance of the SSF. Similar to [16], the reference amplifier path also utilizes active/guard SSF switching pairs to alleviate signal phase related degradation of the intrinsic CMRR.

The second stage amplifier is a capacitively coupled amplifier with programmable gain. Its ac frequency characteristics determine the high-side and low-side cutoff frequencies of the neural amplifier. The OTA for the second stage amplifier shares the same circuit topology as that in [16]. The combined gain of each channel is 1200 V/V (61.6 dB), but can be further increased to 7200 V/V (77.1 dB) by turning on switches G2 to enable a T-capacitor feedback path [29]. The high gain setting of 77.1 dB would allow the resolution of the 10-bit ADC to be fully utilized. The combined gain can also be reduced to 600 V/V (55.6 dB) for acquiring larger amplitude signals by turning on switches G1. By varying the Miller compensation capacitance of the second stage OTA, the high-side cutoff 3-dB frequency of each amplifier channel can be set to 5.0, 5.5, and 7.3 kHz for the 77.1, 61.6, and 55.6 dB mid-band gains, respectively, without affecting the second-stage amplifier feedback stability.

The amplifier low-side cut-off frequency is adjustable by varying the pseudo-resistors (R_{p1}) in the second stage amplifier. Pseudo-resistors are known to have ultra-high resistance that varies asymmetrically with increased voltage swing applied. This is the main contribution to the signal distortion [33], especially when the output signal swing is large.

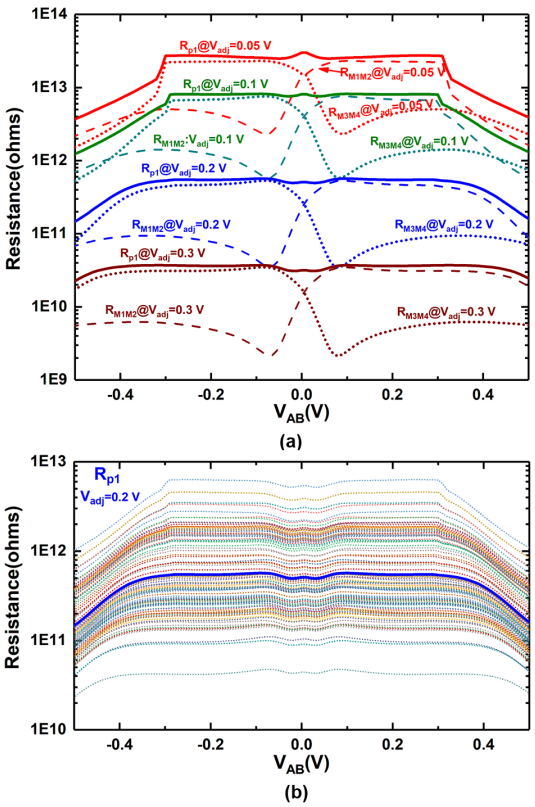

Fig. 3. (a) Simulated resistance–voltage (R–V) characteristics of the pseudo-resistor with four different values of V_{adj}. (b) R–V characteristics of the pseudo resistor for $V_{\text{adj}} = 0.2$ V over 100 Monte Carlo simulations based on statistical process variations.

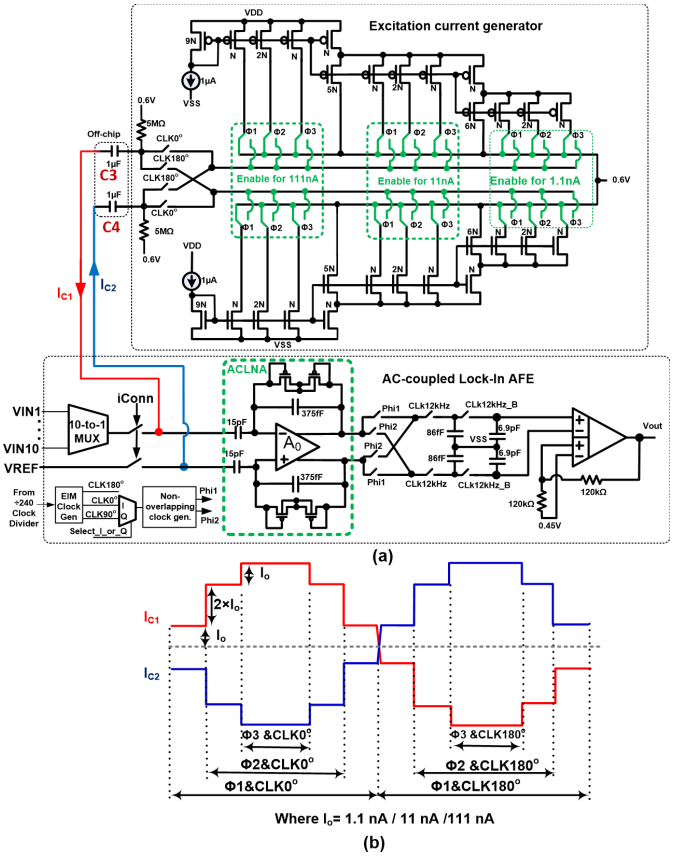

Fig. 4. (a) Electrode impedance measurement circuit. $C3$ and $C4$ are off-chip capacitors. (b) 1 kHz, ten-phase differential excitation current that is generated on-chip for electrode impedance measurement.

One possible solution involves cascading two or more symmetrical pseudo-resistors to increase the output swing [34]. However, this would require at least two inter-N-well spacings and resulting in an increased silicon area. Having more floating N-wells also increases the chance of CMOS latch-up. In this paper, we propose a new pseudo-resistor shown in the lower-right corner of Fig. 2. First, by cascading two pseudo-resistors (M_{p1-2} and M_{p3-4}) and having complementary resistance–voltage characteristics in series as shown in Fig. 3(a), a near constant pseudo-resistance is obtained, even under a voltage difference of +/−0.5 V_p($V_{\text{adj}} = 0.3$ V). Second, this circuit topology only requires two N-wells and one inter-N-well spacing. The lengths of M_{p1} and M_{p4} were sized to be one-third of M_{p2} and M_{p3} to give maximum flatness in resistance across V_{AB}. Monte Carlo simulations revealed that the proposed pseudo-resistor maintains its near constant resistance–voltage characteristics over statistical process corners. This proposed pseudo-resistor implementation results in the neural amplifier having a measured total harmonic distortion (THD) of less than 0.35% for output voltage swings of up to 1 V_{pp} at 1 kHz. An on-chip 4-bit resistor string-based digital-to-analog converter (DAC) (not shown in Fig. 2) provides the digitally adjustable tuning voltage, V_{tune}, for R_{p1}.

Through the SCU, any one of the channel's output can be selectively multiplexed to the input of the analog output driver. This analog driver also drives the on-chip 10-bit ADC and has the same circuit topology as that reported in [16].

B. Electrode Impedance Measurement Circuit

For neural acquisition applications, it is necessary to measure the magnitude and phase angle of each electrode impedance to quantify electrode functionality. Electrode impedance measurement involves supplying a low amplitude sinusoidal current (<1 μA *in vivo*) to flow between a set of signal and reference electrodes. The corresponding voltage response between these two electrodes is acquired using lock-in signal processing [35], wherein the real and imaginary components of the voltage response can be extracted. The magnitude and phase of the complex impedance between the two electrodes can then be calculated from the real and imaginary signal components.

A sufficiently low distortion sinusoidal current stimulus is important for the lock-in amplifier to obtain accurate readings of the real and imaginary components of the voltage response. However, generating a low distortion sine wave is not trivial, and requires high current consumption or additional processing overhead. For example, an 8-bit DAC was used in [36] to generate the sinusoidal current, consumed 120 μA of current, and required large overhead in its communication channel to continuously transmit sine wave coefficients to the DAC.

In this paper, we propose using a stepped current generator that consumes only 12 μA but has sufficiently low-harmonic components for lock-in acquisition. As shown in Fig. 4(a),

the on-chip circuit generates a 1 kHz, ten-phase stepped differential excitation current to flow between a selected signal electrode and the reference electrode. At any instance, only one signal channel can be selected for electrode impedance measurement via a 10-to-1 CMOS multiplexer. The selected channel input and reference input are only connected, via CMOS switches to the EIM circuit when the internal control signal, iConn, is activated by the SCU. This ensures that the neural amplifiers are not affected by the EIM circuit when it is non-operational by default. The stepped waveform is defined by

$$I_{C1}(t) - I_{C2}(t) = \frac{3.232(4I_o)}{\pi} \times \left(\begin{array}{l} \sin \omega t - \dfrac{0.072}{5} \sin 5\omega t - \dfrac{0.072}{7} \sin 7\omega t \\ + \dfrac{1}{11} \sin 11\omega t + \dfrac{1}{13} \sin 13\omega t \cdots \end{array} \right) \quad (1)$$

where I_o is the unit current step of the waveform shown in Fig. 4(b). It can be observed from (1) that the harmonic components of the excitation current until the 11th harmonic is less than -36 dB from the fundamental, closely similar to a sine excitation function. The low-pass filter in the lock-in amplifier would filter out the higher order harmonics. Therefore, the stepped current waveform replaces the need for a power-hungry circuit to generate a low distortion sinewave. A current-ladder scaler [37] allows excitation currents in unit steps of 1, 11, or 111 nA to be generated to target impedances ranging from 1 kΩ to 1 MΩ. The differential outputs of the current generator are weakly biased at 0.6 V_{dc} through on-chip 5-MΩ polysilicon resistors to maintain sufficient voltage compliance for the current sources and sinks.

While the excitation current is flowing between a selected signal electrode and the reference electrode, an ac-coupled lock-in amplifier acquires the corresponding voltage response to extract the in-phase (I) and quadrature-phase (Q) components of the voltage response. The first stage of the lock-in amplifier consists of an ac-coupled low-noise amplifier (ACLNA) with an ac gain of 20 V/V. To save area and power, a single signal demodulator is time-multiplexed to extract the I and Q components at separate instances from the ACLNA's differential output. Both the I and Q components are extracted by switching the demodulation clock phase between 0° and 90°, respectively. A pair of 6.8-Hz low-pass switched capacitor filters extracts the dc component of the differential I/Q signals, and a 4 V/V differential non-inverting amplifier provides the final amplification and conversion to a single-ended output. The dc voltages from the I/Q measurements correspond to the real and imaginary components of the measured electrode impedance. These dc voltages will be digitized by the on-chip ADC, and serially transmitted through the SCU and NIR-LED for calculating the magnitude and phase angle of the electrode impedance off-chip. The EIM block only consumes a total supply current of 20 μA, and the clocks for operating the EIM are derived from the on-chip 3-MHz oscillator.

C. Inductive Power, Data, and Clock Recovery Block

The IPDCR recovers a dc voltage for powering the whole SoC using a self-biased CMOS rectifier [38]. A command data clock is recovered from one of the coil inputs using the clock recovery circuit similar to that in [39]. This recovered clock is divided by 100 times to synchronize the incoming 38.4 kb/s UART data recovered from an ASK demodulator within the same block. The ASK demodulator is a full-wave peak detector circuit coupled with a CMOS comparator, and recovers ASK data with modulation depth of at least 20%.

D. Infrared LED Driver

In this paper, the NIR-LED driver directly receives UART output from the SCU. The driver is composed of a series cascade of five progressively scaled CMOS inverters. The output of the last inverter is connected in series to the first terminal of an on-chip 2-bit programmable resistor. The other terminal of the resistor is connected to the output pad to form a series circuit with the external 850-nm NIR-LED. The NIR-LED's photonic output logic is inverted from that of the SCU's UART output. This eliminates the static current consumption when the internal UART data line remains high due to the SCU remaining in idle mode while awaiting commands from the IPDCR. The external NIR reader circuit would perform the logic inversion of the received NIR data to recover the original output UART data. The programmable resistance can be digitally adjusted using external commands to vary the output power of the NIR-LED. The NIR-LED would be placed subcutaneously (<4 mm depth) [40] when the device is implanted. The capacity to vary the output power of the NIR-LED would help overcome the increased NIR signal attenuation presented by thicker skin tissue and will mitigate gradual tissue encapsulation surrounding the NIR-LED area.

IV. External Inductive Powering Source and NIR Receiver

When implanted, the SoC needs to be transcutaneously powered and controlled through the skin via inductive coupling. At the same time, the digital NIR pulses emitted from the implanted unit need to be acquired via an NIR receiver without interference from the inductive power source. As there are no existing commercial products that can perform both functions simultaneously, we have custom-designed a printed circuit board (PCB) level transcutaneous wireless powering and NIR receiver using commercially available components, as shown in Fig. 5.

The inductive power source comprises a Class-E amplifier [41] (formed by $Q1$, L_{choke}, C_{power}, and L_{power}) generating an ac magnetic field on the on-chip planar coil. L_{power} is formed by a 15 mm, 2.4 μH planar coil on the PCB. A 22-MHz silicon chip oscillator provides the clock for the Class-E amplifier. A carrier frequency of 22 MHz is chosen to allow the recovered clock of the IPDCR to correctly synchronize the incoming 38.4 kb/s UART command while providing sufficient frequency separation from the 7-MHz 3-dB cutoff presented by the low-pass filter within the NIR receiver. This frequency separation helps to reduce the coupling of the

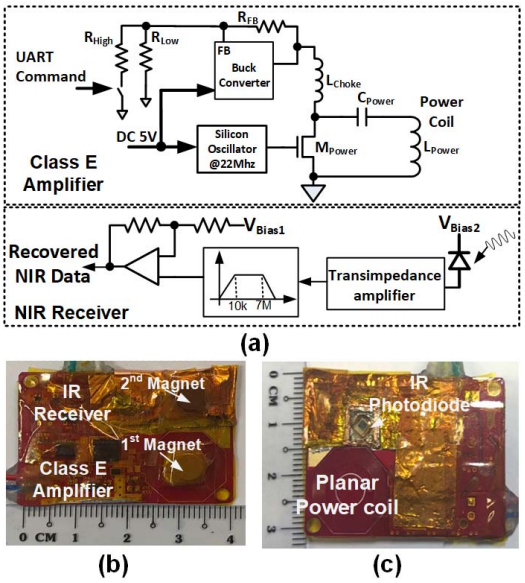

Fig. 5. (a) Circuit schematic of the external powering unit and NIR receiver. (b) Top side of the external recording device. (c) Bottom side of the external recording device.

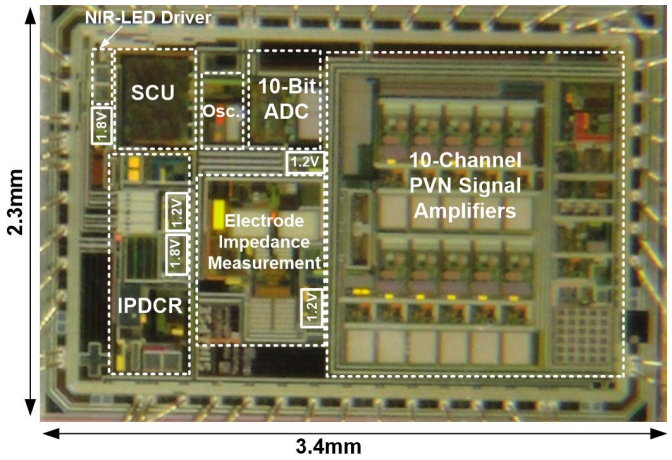

Fig. 6. Microphotograph of the SoC die. CL-LDOs are indicated by solid boxes.

ac magnetic field onto the NIR receiver in addition to the electromagnetic shielding on the PCB board. Transcutaneous attenuation of electromagnetic fields remains minimal even at 22 MHz [42]. To transmit UART commands to the SoC, the incoming UART line digitally modulates the supply voltage of the Class-E amplifier, creating a 20% ASK modulation depth on the generated inductive magnetic field. The SoC IPDCR would then recover the UART commands from the ASK modulated power carrier.

The NIR receiver is based on the circuit described in [23]. It comprises a transimpedance amplifier, gain amplifier, and a window comparator. The transimpedance amplifier converts the NIR data-induced photocurrents into a voltage signal, which is amplified by a second stage amplifier. The second stage amplifier also provided bandpass filtering to reduce thermal noise, and interference from the power carrier. The window comparator derives the full logic level based on the output of the second stage amplifier. As shown in Fig. 5(b) and (c), the NIR receiver circuit is also electromagnetically shielded to significantly reduce interference from the power carrier signal. Two magnets are attached to the top side of the PCB to facilitate alignment with the implant device described in Section V-B.

The data output from the NIR receiver can be acquired by the Intel Edison module, and streamed via WIFI to a computing device for downstream processing and storage. The same module would also issue commands via a separate UART line to the Class-E amplifier for ASK modulation.

V. Measurement Results

The peripheral nerve ENG acquisition SoC was fabricated in a standard CMOS 0.18-μm 1P6M process and measured 7.82 mm^2. The die microphotograph is shown in Fig. 6. For electrical characterization, the SoC was packaged in a QFN40 package. Another SoC was assembled onto a flexible polyimide PCB substrate, along with polyimide-based tf-LIFE electrodes with gold active sites fabricated by SMANIA S.r.l., Pisa, Italy, for *in vivo* PNS experiments. The electrical performance of this SoC and *in vivo* acquisition results are described in Sections V-A and V-B.

A. Electrical Characterization of the SoC

Fig. 7 shows the ac frequency response of the neural amplifier for various gain and low-side cutoff frequency settings. The mid-band gain is approximately 2 dB lower than the designed gain, especially for the 61.6 and 77.1 dB gain settings. This is attributed to the parasitic capacitances introduced by the inputs of the OTAs and interconnects. The high-side cutoff frequencies are measured to be 5.0, 5.5, and 7.4 kHz for the 55.6, 61.6, and 77.1 dB gain settings, respectively, while the low side cutoff frequencies can be digitally tuned from 0.1 to 400 Hz.

Fig. 7 also shows the input referred noise power spectral density (PSD) of the neural amplifier. Even though the neural amplifier noise level is determined primarily by $1/f$ noise, the integrated input referred noise level, for signal bandwidth of 10 Hz–5.5 kHz still measures 1.9 μV_{rms} (12.5 μV_{pp} for $\pm 3.3\ \sigma$), meeting the requirements for peripheral nerve ENG acquisition. With an effective current consumption of 16.3 μA for each neural amplifier channel (including CCLNA, SVF and second stage amplifier), the noise efficiency factor (NEF) and power efficiency factor (PEF) for the neural amplifier is 4.0 and 19.2, respectively. The measured tuning range of the low-side 3-dB cutoff frequency is shown in Fig. 8 for four different chips. A worst-case variation of $+/-24\%$ variation in cutoff frequency originating from transistor process variation was observed across the tuning range.

The intrinsic common mode rejection ratio (ICMRR) was characterized using a 100 mV_{pp} common mode test signal and measured at least 75 dB up to 1 kHz.

The ADC was characterized while clocked by the on-chip oscillator and powered by its on-chip LDO. The ADC's 10-bit output was serialized by the SCU along with start and end

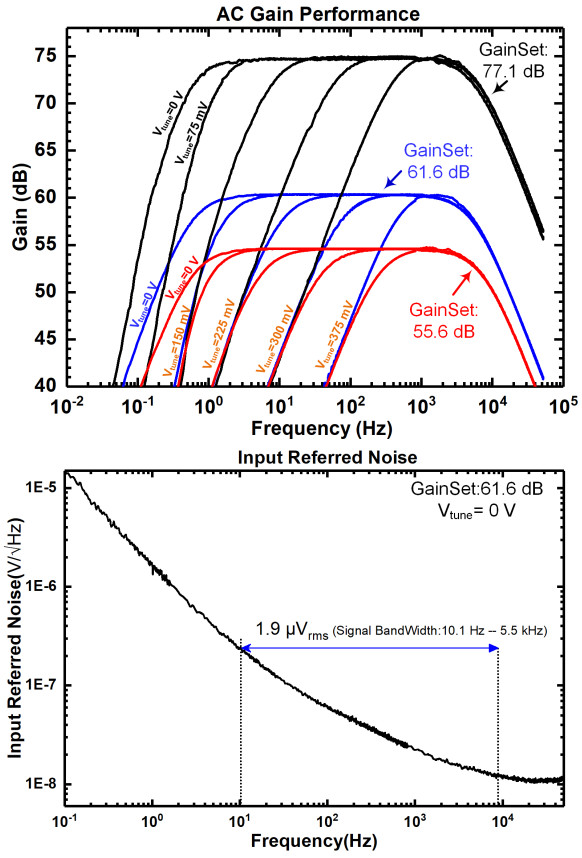

Fig. 7. AC frequency response with different gain settings and low-side cutoff frequency settings. Lower graph shows the input referred noise PSD of one channel of the PNS amplifier.

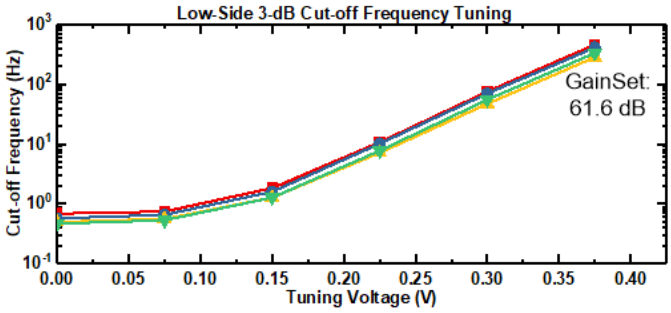

Fig. 8. Tuning range of the low-side 3-dB cutoff frequency of one amplifier channel.

frame markers for a ten-channel multiplexing operation, giving an effective sampling frequency of 17.85 ks/s. For an input swing of 1.11 V_{pp} at 1 kHz, the ADC has an ENOB of 8.1 bits.

The EIM circuit was characterized using complex impedances, each formed by a resistor in series with a capacitor. Summarized in Table I, the measured impedances using the EIM circuit were benchmarked against those obtained with an Agilent 4294A precision impedance analyzer. The electrode impedance circuit exhibited less than 10% magnitude error, and less than 8° phase angle error when measuring complex impedances from 1 kΩ to 1 MΩ.

TABLE I

IMPEDANCE MEASURED BY A PRECISION IMPEDANCE ANALYZER VERSUS THOSE MEASURED BY THE SOC

Agilent 4294A Precision Impedance Analyser		This work	
Magnitude(Ω)	Angle(Degrees)	Magnitude(Ω) / (%Error)	Angle(Degrees) / Error(Degrees)
934	-72.5	906 / -3.0	-66.7 / +5.7
1052	-48.4	968 / -7.9	-41.6 / +6.8
997	-23.9	932 / -6.5	-26.5 / -2.6
9852	-74.8	9884/ +0.3	-78.7 / -3.9
10187	-46.9	9813 / -3.7	-46.0 / +0.9
9680	-22.3	9601 / -0.8	-21.2 / +1.1
101813	-72.0	102878 / +1.1	-74.9 / -2.9
100335	-45.9	103793 / +3.5	-46.1 / -0.1
101143	-27.8	105660 / +4.5	-26.6 / +1.2
917600	-76.1	850269 / -7.3	-78.8 / -2.7
1015500	-46.5	918388 / -9.6	-52.2 / -5.7
1012800	-28.8	945377 / -6.7	-36.7 / -7.9

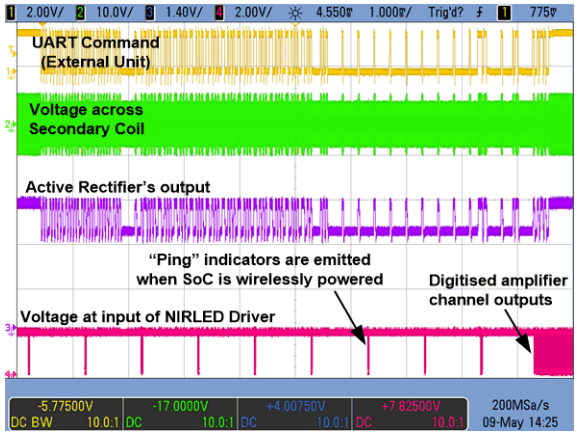

Fig. 9. SoC operating node voltages when it was inductively powered while a command to probe the on-chip analog power supply rail was issued.

Fig. 9 illustrates the operation of the peripheral nerve ENG acquisition SoC while it was inductively powered by the external unit described in Section III. A PCB planar coil of the same dimension and inductance as that of the external unit was connected to the antenna inputs of the SoC. A 22-pF capacitance was connected in parallel with the PCB coil to ensure resonance power coupling with the primary coil. An air gap of 2.4 mm was maintained for this and subsequent measurements of this section. In this setup, a UART command was sent to the external unit, which produced a corresponding ASK modulation on the 22-MHz magnetic field. The IPDCR circuit within the SoC successfully decoded the ASK modulated data on the power carrier and activated serial digitization of each output of the neural amplifier. The serialized neural data stream was then sent to the NIR-LED driver.

For a rectified input voltage of 2 V, the SoC consumed 2.3 mW, while ten channels of digitized data were serially transmitted to the NIR-LED at 3 Mb/s. The NIR-LED dissipates 2.1 mW. Therefore, the total power consumption of both the SoC and NIR-LED is 4.4 mW. Fig. 10 shows the power breakdown of the SoC. We have also established that

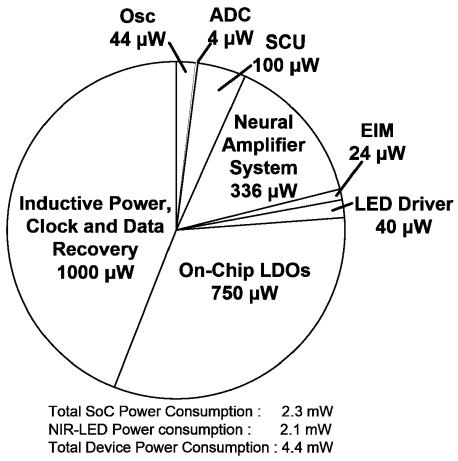

Fig. 10. SoC Power breakdown chart.

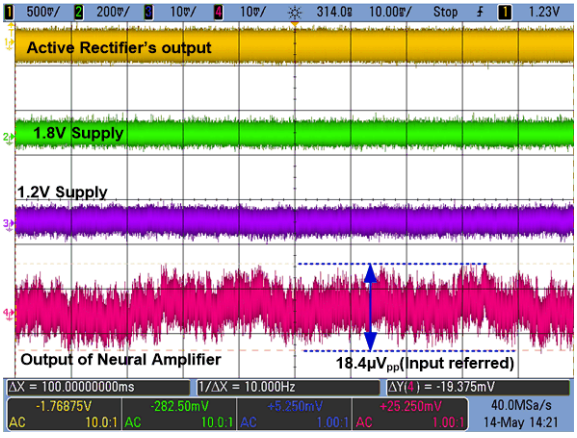

Fig. 11. On-chip supply rail and amplifier output voltage when the SoC was inductively powered. All oscilloscope channels are ac-coupled (high-pass filtered at 3.5 Hz by the oscilloscope).

only 30 mW needs to be supplied to the Class-E amplifier to inductively power, through a piece of 2.4 mm thick saline soaked paper, the implantable SoC for successful NIR data transmission.

Fig. 11 shows the peak-to-peak voltage levels of some nodes on the SoC, while it was inductively powered. One of the neural amplifier channel's output is also included. The neural amplifier's gain and low-side 3-dB cutoff frequency were configured to 61.6 dB and 10 Hz, respectively. Therefore, the peak-to-peak input referred noise level of the neural amplifier was calculated to be 18.4 μV_{pp}. The 5.9 μV_{pp} increase in input referred noise level above that measured in static dc condition (12.5 μV_{pp}) was attributed to inductively coupled noise while the SoC was wirelessly powered.

The on-chip 3-MHz oscillator had a period jitter of 5.53 ns_{pp} as measured using a real-time digital oscilloscope. The same clock signal was transmitted via NIR-LED to the external unit, and the received clock period jitter measured 6.21 ns_{pp}. The received clock's period jitter was only 1.9 % of the 3-MHz clock period. This was lower than the ± 2 % frequency error required for reliable UART data communication. Further investigation revealed that the reference voltage node of the

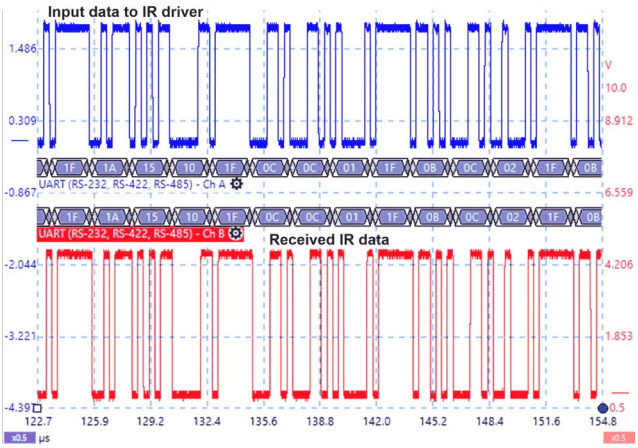

Fig. 12. UART data streaming into the NIR-LED driver (top) and corresponding UART data received at the external receiver (bottom).

relaxation oscillator is unable to sufficiently reject supply voltage ripples originating from the SCU. Circuit simulations revealed that the clock jitter can be further reduced to 1.9 ns_{pp} by adding an 8 pF decoupling capacitance to the reference voltage node and introducing local decoupling capacitors to the oscillator bias generators in the next chip revision.

A Picoscope 3406D was utilized to decode the UART data input and the data received from the external unit to the NIR-LED driver. As shown in Fig. 12, the measured UART data at the output of the NIR receiver matched that of the transmitted UART data. We observed that for a run time of 51 s (corresponding to 7 232 472 bits of received NIR data), there were no received bit errors. Hence, the BER was $<4 \times 10^{-7}$ at the 95% confidence level.

The performance parameters of this SoC are summarized in Table II and are comparable to other state-of-the-art CNS and PNS SoC implementations.

B. In Vivo Experimental Results

An *in vivo* transcutaneous acute peripheral nerve ENG acquisition was performed with the SoC on a Sprague-Dawley rat. The experiment was performed in accordance with the protocol approved by the Institutional Animal Care and Use Committee (IACUC) of the National University of Singapore.

Fig. 13(a) shows a pre-encapsulated device with an SoC assembled along with four 0402-sized capacitors onto the right section of a 0.1 mm flexible polyimide PCB substrate. A planar coil of the same design as that of the external receiver and an NIR-LED was fabricated on the left section of the PCB substrate. Two magnets were also attached underneath the PCB to ensure good coil and optical alignment with the external unit. Each magnet weighs 0.39 g and has a diameter of 6.4 mm and thickness of 1.6 mm. Both sections of the PCB are interconnected with a flexible PCB bridge. The right section of the PCB can be further miniaturized by replacing the QFN package with direct chip-on-board packaging techniques in the future.

Prior to the experiment, a tf-LIFE electrode was soldered onto the input pads of the PCB assembly. To prevent the

TABLE II
COMPARISON OF SoC WITH STATE-OF-THE-ART WORKS

Parameters	**This work**	[30] **JSSC'14**	[31] **TBCAS'16**	[17] **TBCAS'17**	[11] **Nat.SR'18**
Application	Peripheral ENG Only	Cortical ENG + Stim.	Cortical ENG + Stim.	EMG + Stim.	Peripheral ENG + Stim.
Process Technology(nm)	180	180	180	180(HV)	130
Die Size(mm^2)	7.82	7.29 (include I/O pads)	7.74	25.08	20.0▲
Die Size(mm^2) without Stimulator and with up to 10-amplifier channels	7.82	7.02	6.69	17.2	16.45
Implant Device Size(cm^3), Weight (g)	3.4 , 3.9	–	–	0.5# , 0.7#	2.25 , 2.8
***In vivo* test**	Implanted	–	Non-implant	Implanted	Implanted
Powering scheme	22 MHz Inductive	915 Mhz Far-field	10 MHz Inductive	2 MHz Inductive	13.56 MHz Inductive
Output telemetry	Near Infrared	Back-scattering	RFID-LSK##	RFID-LSK##	RF 433Mhz
Output Data rate (Mbps)	3	0.8	2	2	9
Telemetry BER	$<4x10^{-7}$*	–	–	$<10^{-3}$	–
No. of recording channels	10	4	8	16	32
Mid-band gain (dB)	54.6/60.3/75	54	60/74	40-62	51.6/76
Low side 3-dB cutoffs(Hz)	0.1-300	0.64	0.06 -0.5	5 -500	20
High side 3-dB cutoff(Hz)	5.5 k	6k	500 -3k	500 – 7 k	15 k
Input referred noise (μV_{rms})	1.9	6.3	1.97	7.68	3.0
NEF, PEF	4 , 19.2	3.76 , 25.4	2.9 , 8.41	7.64 , –	2.95 , 8.68
Sample rate (Ksps/Channel)	17.85**	25	80	4	25
ADC Resolution , ENOB (bits)	10, 8.1^	8 , 5.6	8, 6.5	10, 8.5	10, –
Electrode Impedance Measurement	Yes	No	No	Yes	No

#Before Encapsulation. ##Load-Shift Keying. *With 95% Confidence level. **For 10 channels.
^For 17.85 ksps on 10 channels. Signal frequency at 1 kHz. ▲2 Die solution

ingress of body fluid, the assembled PCB was first encapsulated with the Smooth-On Body Double fast-set silicone, followed by biocompatible Kwik-Sil silicone. To provide an opening for NIR transmission, the NIR-LED was encapsulated only with the Kwik-Sil silicone. The final encapsulated device shown in Fig. 13(b) weighed 3.9 g. The bulk of the device weight comes from the silicone encapsulation. The encapsulated device package consists of the coil on one end and the electrode pads reaching toward the sciatic nerve on the other end. The former would be implanted in the subcutaneous region (below the skin) to ensure that the power and acquired data are harvested efficiently from and transmitted reliably to the external unit. The latter would also be situated close to the sciatic nerve region to ensure that the ENG signals would be acquired while minimizing electrical artifacts and electromagnetic interference. As such, while the PCB consisting of both aforementioned sections post-encapsulation spans a total of 5.9 cm in length and the coil measures 2 cm, the overall device package takes up only 3.4 cm^3 in volume with a maximum thickness of 1 cm. The total device power dissipation per unit volume would be 1.3 mW/cm^3, which is well below the 40 mW/cm^3 limit, so as to prevent a catastrophic increase in 2 °C for most body tissues [43].

During the experiment, the rat was anesthetized with a mixture (0.2 ml/100 g) of ketamine (75 mg/kg) and xylazine (10 mg/kg) injected intraperitoneally (IP), and subsequently maintained with hourly IP injections (0.1 ml/100 g). Body temperature was maintained at 37 °C using a heating pad, and surgical procedures were carried out to expose the left sciatic nerve. The encapsulated device was placed subcutaneously (with rat skin thickness of 2 mm) over the left back area and the tf-LIFE electrode was implanted in the left sciatic nerve [Fig. 13(c)]. The implant device was then transcutaneously powered using the external unit. An Intel Edison module was used to issue UART commands to the implant through the external unit, and to forward the received NIR data via WI-FI wireless interface to a laptop computer for storage and post processing using MATLAB (by MathWorks). The gain and low-side 3-dB cutoff frequency of all amplifier channels was set to 77.1 dB and 10 Hz, respectively. The left hind foot of the rat was then flexed manually toward the rat's belly 11 times per recording to evoke action potentials (AP) associated with proprioceptive feedback during flexion. The acquired APs correlated with limb flexion, as shown in the signal presented for the first trial in Fig. 13(e). Some artifacts arising from micro-movements in the wire connection between the tf-LIFE electrode and the acquisition device were observed between 3.3 and 3.8 s [indicated by the vertical arrows in Fig. 13(e)]. The baseline noise level was less than 25 μV_{pp}, and was close to the electrically characterized peak-to-peak noise level.

Fig. 14(a) shows the ENG waveforms for all the 11 trials performed during the same acquisition session as Fig. 13(e). The signals were band limited between 300 Hz to 3 kHz for better observation of the evoked APs. The baseline noise level was less than 25 μV_{pp}, while the evoked APs had amplitudes up to 90 μV_{pp} when the rat's hind foot was maximally flexed. A magnified view is provided in Fig. 14(b) to show the presence of individual spikes for channels 7 and 8. Using SpikeTrain from Neurasmus B.V, the time-averaged spikes from channel 8 are summarized in Fig. 14(c). Two distinct AP clusters were observed in Fig. 14(c). This *in vivo*

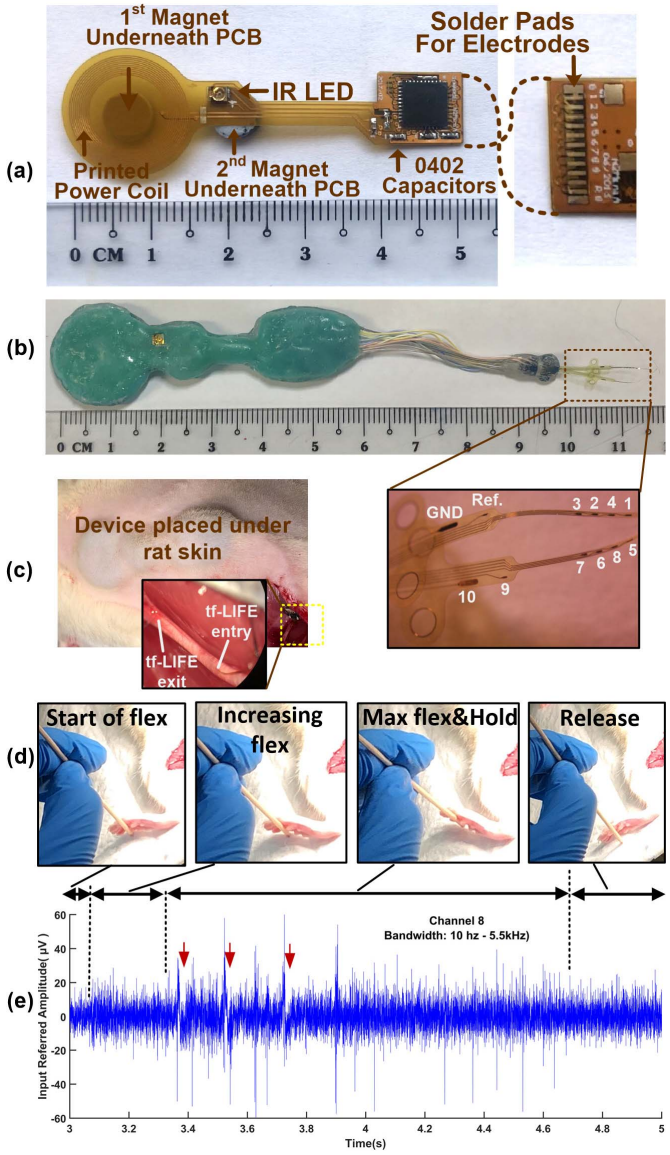

Fig. 13. (a) Polyimide PCB populated with the SoC and other components prior to electrode attachment and encapsulation. (b) Encapsulated device prior to acute implant (with magnified view of the electrode mapping to the SoC input channels). (c) Device placed subcutaneously and tf-LIFE electrode secured on the sciatic nerve during the acute animal experiment. (d) Sequence of one trial involving the rodent hind foot being flexed and then released. (e) Corresponding evoked APs acquired by the SoC. The arrows indicate the occurrence of wire movement artifacts.

experiment demonstrated the sensitivity of the peripheral nerve ENG acquisition SoC and its low noise acquisition capability when used with intraneural electrodes while being inductively powered and performing transcutaneous NIR data telemetry.

Using the on-chip EIM circuit, the measured impedance (at 1 kHz) between the signal electrodes and reference electrode ranged from 180 kΩ (channel 10) to 350 kΩ (channel 8). The phase angles were at most −70°, which confirmed the near-polarizable characteristic (strong capacitive effect) [44] of the gold metal used as active sites in the tf-LIFE electrode. It was also found that channel 9 exhibited high impedance (>1 MΩ) and high input referred noise levels (>100 μV_{pp}), indicating poor electrode contact to the nerve tissue. This channel was excluded from subsequent analysis.

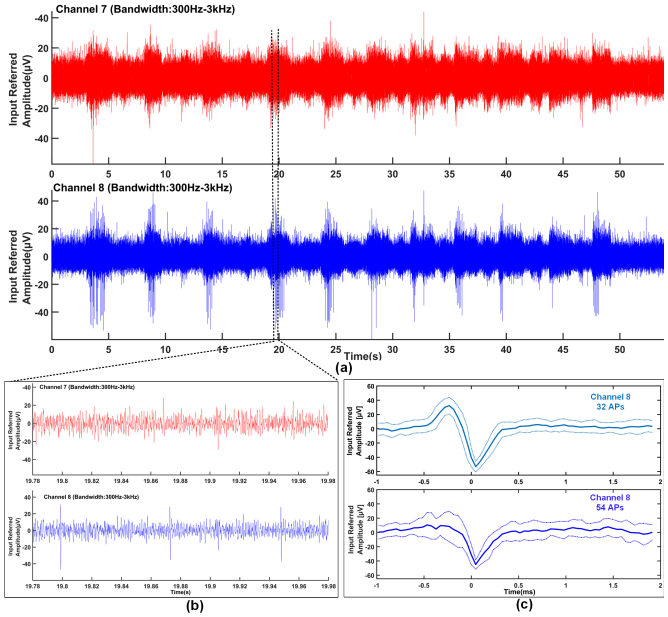

Fig. 14. (a) ENG signals from channels 7 and 8 over 11 trials. (b) Zoomed-in view of the waveforms. (c) Averaged APs for channel 8 over all 11 trials with 95% confidence interval.

VI. Conclusion

A wirelessly powered, ten-channel peripheral nerve ENG acquisition SoC has been validated. Fabricated on CMOS 0.18-μm technology, this 7.82 mm^2 SoC-integrated inductive power, command and clock recovery circuits along with neural amplifiers, 10-bit ADC, digital control engine, and NIR telemetry on a single die. This SoC also features *ad hoc* electrode impedance measurement function for each channel. Each neural amplifier channel exhibited 1.9 μV_{rms} input referred noise and therefore an NEF (PEF) of 4 (19.2) for a signal bandwidth of 10 Hz–5.5 kHz. While transcutaneously powered using inductive coupling, all digitized neural data can be sent wirelessly to an external receiver via NIR telemetry at a rate of 3 Mb/s (17.85 ks/s/channel) while consuming 4.4 mW. This SoC was assembled along with only four SMD capacitors, one power coil and one NIR-LED in a fully wireless implantable peripheral nerve ENG acquisition device. This device was successfully implanted and validated *in vivo* for the acquisition of evoked proprioceptive APs from the sciatic nerve of an anesthetized rat.

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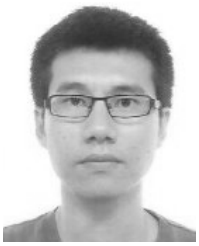

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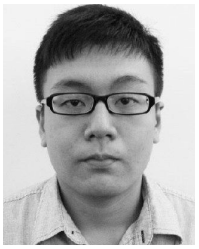

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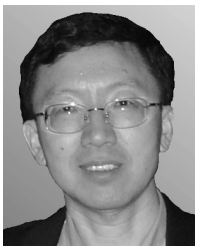

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