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Technical Note

Deposited poly-Si as on-demand linewidth compensator for on-chip Fabry–Perot interferometer and vertical linear variable optical filter bandpass and passband manipulation

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Abstract

Deep reactive ion etching (DRIE) is an important process for etching vertical structures for microelectromechanical systems. Due to the sidewall profile of some photoresists as well as effects from upstream processes, bulk micromachined structures, to a certain extent, could differ from expected. Concerning photonics applications, minute deviations from the intended design might alter its optical characteristics. The most popular approach is to introduce a compensation factor during mask design. However, such a method is not robust enough to accommodate batch variations due to varying process conditions.

In one particular example specific to this work, the simulated passband for a Si-air Fabry–Perot interferometer configuration was 3.67 μm. However, post DRIE the passband was measured to be 3.40 μm. To resolve this discrepancy, linewidth compensation using low-pressure chemical vapor deposition (LPCVD) poly-Si is presented. When 170 and 194 nm of poly-Si were separately deposited, the passbands redshifted to 3.54 and 3.57 μm, respectively. With the LPCVD poly-Si layer being highly conformable, the full width half maximum remains unchanged at 80 nm. An on-chip linear variable optical filter was demonstrated with a compensation of 194 nm poly-Si. It was observed that the working range redshifted from 3.0–3.9 μm to 3.3–4.5 μm.

Keywords: LVOF, Si-air, Fabry–Perot, optical filter, linear variable filter

(Some figures may appear in colour only in the online journal)

Introduction

The deep reactive ion etching (DRIE) technique was developed in the early 1990s as an alternative to silicon (Si) wet

etching for bulk micro-machining [1, 2]. The technique offers a highly anisotropic vertical etch profile which does not depend on crystal orientation. Thus, DRIE offers excellent pattern transfer capability [3]. Due to its many advantages, DRIE revolutionized the way microfabrication was previously performed. Being an 'IC compatible' process, it gives rise to

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new possibilities for the fabrication of micromechanical electrical systems (MEMS) and micro-optomechanical electrical systems (MOEMS) devices. Some of these examples include MEMS accelerator [4], gyroscope [5], cantilever [6], Fabry–Perot interferometer (FPI) [7] and linear variable optical filter (LVOF) [8]. In particular, deep etched on-chip FPI and LVOF have been demonstrated by various groups around the world [7, 9, 10]. Basically, they are constructed by sandwiching a cavity consisting of a pair of either metallic or dielectric Bragg reflectors (DBR). Passband selection is dependent on the cavity distance between the DBRs. For FPI, the distance between the DBRs is fixed while the cavity distance varies linearly along the length for LVOF.

Although DRIE is anisotropic in nature, one grave concern is the issue of linewidth deviation from the original design [11]. This is particularly important for microfabrication of optical components such as micromirrors, in-plane optical filters, etc. One specific example is the case of on-chip optical filters where bandpass or bandstop depends on linewidth/spacing [12], delineation could cause transmission peaks to red or blue shift. Linewidth deviation phenomenon could be attributed to the following reasons: (1) improper photoresist lithographic process, and (2) utilization of under-optimized DRIE recipe. Ideally, developed photoresists will form vertical sidewalls on the patterned substrates. In reality, positive toned resists might form a positive slope after being subjected to hard bake conditions [13]. This results in less resist volume to protect the pattern edges. Over time, exposed Si at the edges is subjected to etching which causes Si removal. Eventually, Si linewidth decreases as the etching prolongs. To address this issue, Saadany *et al* proposed the concept of linewidth compensation during the mask design stage based on the feedbacks gathered from previous optical measurements [14]. Such an iterative nature could prove to be costly and time-consuming as it concerns multiple masks fabrication and various designs have to be experimented on. The challenge is exacerbated when a structure has features consisting of different linewidths.

One method to mitigate Si loss is to 'patch up' using a material with similar properties. In the particular case of Si, poly-Si appears to be the material of choice. Previously, low-pressure chemical vapor deposited (LPCVD) poly-Si, doped and un-doped, were primarily developed for the fabrication of deep trench poly-Si [15]. Such works placed a huge emphasis on creating void-less structures primarily for use in Si interconnections [16]. In this communication, we showcased the use of LPCVD un-doped poly-Si as a compensation agent for the loss of linewidth incurred during DRIE for the fabrication of Si/air FPI and LVOF. Furthermore, we demonstrated that by manipulating poly-Si deposition thickness, one can tune the passband at will.

Methodology

On-chip optical filters such as FPI and LVOF were simulated using the Lumerical FDTD software [17]. In the FDTD window, plane wave was selected as the preferred source shape and incidence angle was set to 0°. Amplitude was set to 1.0 while the wavelength range was fixed from 2.5 to 5.0 μm. Si and air were identified as suitable high refractive index [H] and low refractive index [L] layers respectively. Alternating layers of Si and air were simulated in the following configuration: [HLH]—cavity gap—[HLH]. Thereafter, FPI structures (materials) were drawn with the following dimensions: 1.45 μm (Si, Palik), 1.00 μm (air) and cavity of 1.70 μm (air). Refractive indices specified by FDTD during simulation were 3.43 for Si and 1.00 for etched space. Subsequently, the required Si pillars were then fabricated in a three-step process as illustrated in figure 1.

Electron beam lithography (EBL) was performed as follows: Si wafers were cleaned in acetone followed by isopropanol under ultrasound agitation. Thereafter, the wafers were spin coated with SU-8 2000.5 for 5 s at 500 rpm and 30 s at 2000 rpm to obtain a resist of approximately 700 nm thick. The wafers were soft baked for 1 min at 95 °C on a hotplate. Subsequently, 3 mm long patterns with a linewidth of 1.45 μm were written using JBX-6300fs (JEOL). The acceleration voltage was set to 100 kV with a dose set to 5.5 μC cm^{-2}. FPI DBR pillars were written parallel to each other. In the case of LVOF fabrication, one set of DBR pillars were tilted 0.0191° with respect to the other set of DBR. The DBRs were spaced 1.5 μm and 2.5 μm at the shortest and longest ends respectively. Thereafter, post-exposure baking was performed at 95 °C for 1 min. The wafers were then developed in an SU-8 developer for 60 s. Finally, the wafers were hard baked at 200 °C for 30 min on a hotplate.

Patterned samples were then DRIE etched with the resist as a hardmask. DRIE was performed on the PlasmaPro 100 Estrelas (Oxford Instrument). During the etching cycle, the SF$_6$ flow rate was set to 300 sccm for 200 ms at 2000 W. During the passivation cycle, C$_4$F$_8$ was set to 200 sccm for 200 ms at 2000 W. The etch and passivate cycles were repeated for 200 times. A chamber pressure of 120 mTorr was maintained throughout the Bosch process. To ensure etching consistency, the DRIE chamber was cleaned after every tenth etch. The Si to resist etch selectivity was found to be approximately 60:1.

LPCVD poly-Si was deposited in model 1218 four-stacked furnace (MRL Industries) at 625 °C. The furnace was evacuated to achieve a base pressure of 12 mTorr. Thereafter, SiH$_4$ gas was continuously charged into the chamber at a flow rate of 25 sccm and poly-Si deposition was conducted at a chamber pressure of 250 mTorr. A deposition rate of approximately 10 nm min^{-1} was achieved.

Characterization

During the developmental process, samples were carefully sectioned using diamond tip scriber for cross-sectional analysis performed on a field emission scanning electron microscope (FESEM, LEO). Primarily, FESEM was used to assess the verticality of the etched structures. For clear visualization, linewidth thickness and DRIE scallops were imaged at high magnification. X-ray diffraction (XRD) was performed using D8 Advance diffractometer (Bruker). The
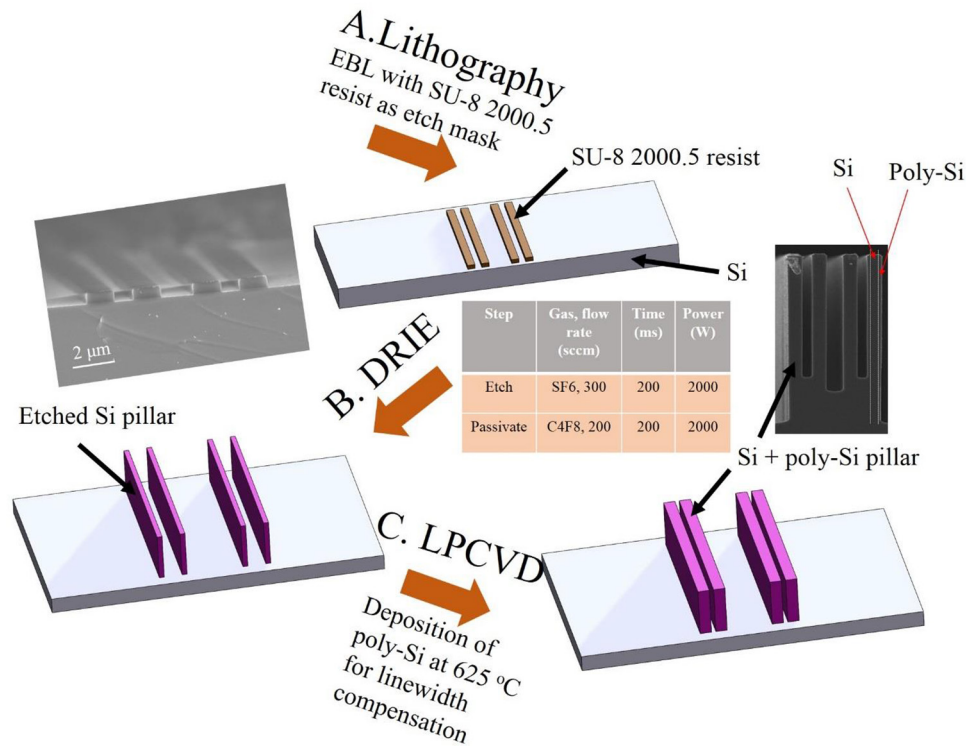
Figure 1. Fabrication steps to construct on-chip Si-air pillars for FPI as well as deposition of poly-Si as linewidth compensator to change the fabricated Si linewidth. (A) fabrication of designed linewidth by EBL (inset: scanning electron microscope (SEM) image of hard baked SU-8 2000.5), (B) DRIE and etching recipe for high aspect ratio structures and (C) compensated structures by LPCVD poly-Si deposition with SEM image showing the final etched structure. Two white lines were drawn on one pillar to discriminate Si from deposited poly-Si. Similar fabrication steps were used to fabricate LVOF with the exception that one set of DBR was scribed at an angle of 0.019° with respect to the other DBR during EBL.

x-ray source was Cu-Kα with the corresponding wavelength of 1.541 Å. 2θ was scanned from 20°–80° with steps of 0.02°. The D8 Advance was operated at 40 KV and 40 mA in the detector-scan mode with the slit set to 1 mm and theta set to 1°. Raman spectroscopy was carried out on a UHTS300 (Witec) spectrometer. The sample was focused using the attached 100× objective lens and the grating groove density was set to 1800 g mm^{-1}. The sample was illuminated using a 532 nm excitation laser. Ellipsometry was performed on the poly-Si deposited SiO$_2$/Si wafer monitors using IR-VASE (J A Woollam) from 1.7–37.0 μm with an angle of incidence set to 55° and 65°. During modeling, the option for surface roughness was enabled. Since the poly-Si layer is thin, poly-Si was modeled directly on top of the SiO$_2$ layer. In this case, a multilayer model was set up in the following order: Roughness—Poly-Si–SiO$_2$–Si substrate. Curve fitting was performed from 333 to 5900 cm^{-1} with scanning steps of 7.7 cm^{-1}. In this case, a mean square error of 4.936 was achieved. Atomic force microscopy (AFM) scanning was performed using the NX-20 (Park Systems) with an AC160 tip. The sample was firmly mounted onto a 5° tilted stage to reveal as much surface area as possible on the outermost pillar. The cantilever was programmed to scan the surface along the height of the pillar. Fourier transform infrared (FTIR) measurement was carried out on a Cary 660 FTIR with a microscope unit of Cary 600 (Agilent). Fabricated samples were vertically mounted onto a customized stage which was secured onto the

sample stage for measurement. The aperture size was fixed at 100 μm × 20 μm and the resolution set to 16 cm^{-1}. The wavelength was swept from 2.5–5.0 μm in transmission mode with the background taken in air. Experimentally gathered data were then compared to the data from the simulation.

Results and discussion

DRIE is the most popular tool for etching a multitude of substrates. Si is considered to be the most popular choice. In many instances, in order to obtain the desired etch profile, one has to optimize the etching recipe which involves iterating gas flow as well as alternating etch/passive time and ratio. Moreover, to complicate the matter, etch characteristics might vary between different batches, given a slight change in chamber condition from one batch to another. This could potentially attribute to different outcomes. To minimize such equipment error, a chamber cleaning recipe was performed after every tenth etch.

For the design of Si-air DBR as the mirror for FPI, alternating layers of high and low refractive index materials were needed. In this case, Si pillars constitute the high refractive index layer [H] while air spaces constitute the low refractive index layer [L]. In this case, the FPI comprises of two Si-air DBR stacks sandwiching an air cavity. The general design rules for the FPI quarter-wave stack equation (1) and half-wave stack equation (2) are as follows:
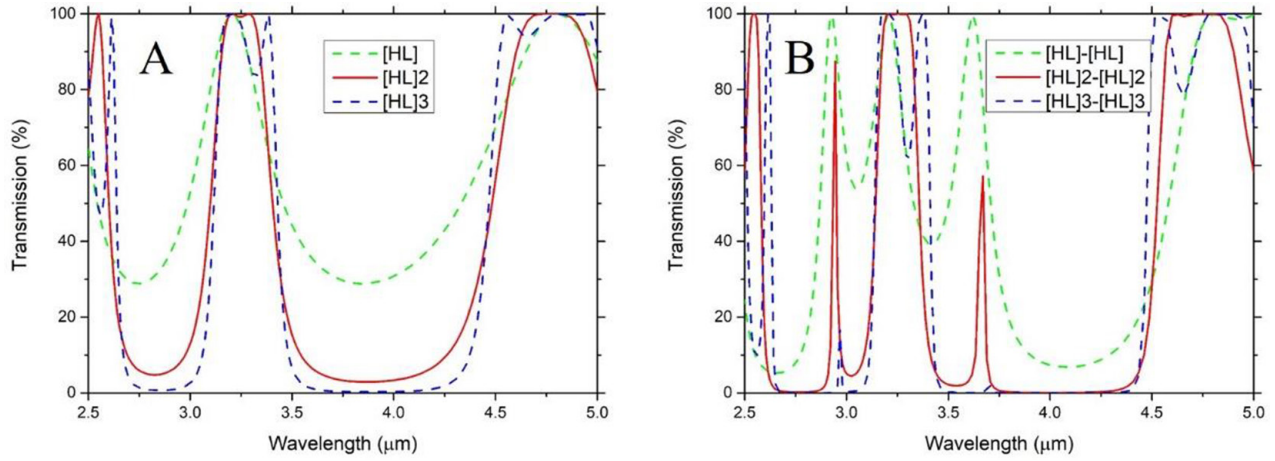
Figure 2. (A) Simulated Si-air DBR profiles for 3.3–4.5 μm effective wavelength range showing a direct correlation of better mirror quality with an increase in numbers of [HL] pairs. (B) Effects of the number of [HL] pairs DBR sandwiching air cavity of 1.7 μm gap on passband intensity and full width half maximum (FWHM).

$$n \cdot t = \frac{m\lambda}{4} \quad (1)$$

$$n \cdot tc = \frac{m\lambda}{2} \quad (2)$$

where n is the refractive index, t is the thin film thickness, tc is the cavity gap, m is the propagation mode and λ is the center passband.

From the FDTD simulation, as shown in figure 2(A), $[HL]^2$ DBR is sufficient for FPI with well-marked transmission passband and band stops. Although increasing the numbers of [HL] is desirable, the transmission passband intensity would be compromised as shown in figure 2(B). In order to preserve high passband intensity and acceptable full width half maximum (FWHM), fewer layers of [HL] would be preferred at the expense of sloped band stops. As such, all subsequent simulations and devices would be fabricated using the $[HL]^2$ configuration.

One potential issue of deep etching is linewidth deviation from its intended design [18]. A myriad of upstream processes could potentially contribute to this problem; it is largely manifested by the presence of DRIE scallops which undercut into the Si pillar sidewall. The issue is further accentuated by the erosion of photoresist during DRIE which results in additional removal of sidewall material. Such delineation from simulated design is critical, especially for photonics applications. In the case of FPI and LVOF, slight deviations could result in the shifting of passbands. The worst case scenario would be a total attenuation of the signal [19]. It is worthwhile to note that the nonvertical etch caused by an under-optimized recipe could also potentially lead to low signal to noise ratio as well as a significantly enlarged FWHM. In this communication, rectification steps for non-vertical etchings will be excluded. The solutions are well discussed in the literature [20].

FESEM images of the deep etch FPI structures are shown in figure 3. As shown in figure 3(A), the total etch depth achieved was approximately 16.0 μm while the shallowest etch depth was approximately 12.5 μm deep. The difference in the etched profile could be attributed to the RIE lag effect. This effect could be rectified by using SOI wafers, where buried oxide would act as a stop etch layer. The measured widths of the freshly etched sample are approximately 1.25, 1.20 and 1.90 μm for Si, air space and cavity gap respectively. At a higher magnification, as shown in figure 3(B), visible DRIE scallops could be observed. The scallops were formed as a result of etching and passivation steps cycling. Scallop pitch of 80 nm and amplitude of approximately 30–40 nm were measured. It was proven previously that the presence of scallops could contribute to an optical signal attenuation [21]. The initial break, as observed directly beneath the SU-8/Si interface contributed most significantly to linewidth loss. On the other hand, the positively sloped resist can be visualized in figure 1(A) (Inset) and figure 3(B). This is a result of SU-8 low contrast nature [22] Also, SU-8 was affected by acid-loss effect due to alkaline contamination incurred during handling [23]. Furthermore, the formation of scallops further decreased the Si linewidth on both sides of the pillars. As depicted in figure 3(C), poly-Si was deposited conformally on all surfaces with an optimized LPCVD deposition recipe. As a note, the gain in Si linewidth was proportional to the decrease in air linespace. Moreover, as shown in figure 3(D), DRIE scallops were less distinct after the LPCVD poly-Si deposition process.

To illustrate the characteristics of the deposited poly-Si layer, the following experiment was conducted. A sample was cleaved after every step to reveal the profile. Deep-etched Si-air FPI structures as shown in figure 4(A) were dry oxidized at 950 °C for 30 min in order to allow the growth of a thin layer of SiO_2. The SiO_2 layer was measured to be approximately 100 nm thick. The latter is shown in figure 4(B). The insulator layer was intentionally fabricated to distinguish the bulk Si from the deposited poly-Si. This was used to visualize the nature of the deposited poly-Si thin film. Subsequently, the sample was subjected to LPCVD with SiH_4. Finally, the completed structure is shown in figure 4(C). Comprising a layer of SiO_2 and poly-Si as indicated in figure 4(D), the thickness of the poly-Si was measured to be 87 nm on each side of the
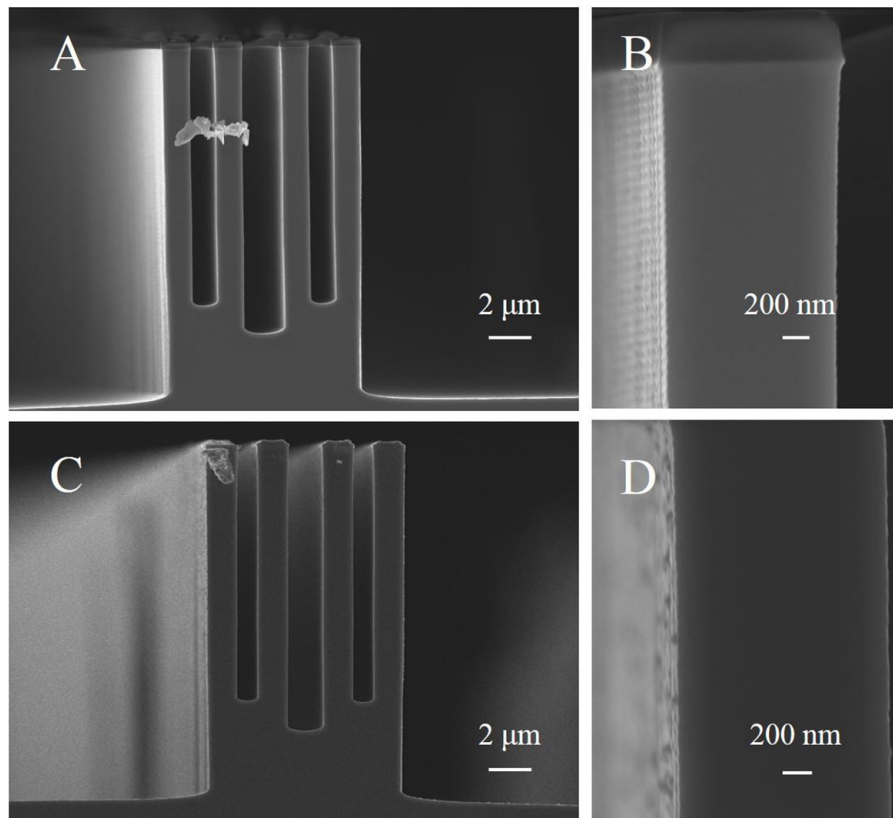
Figure 3. SEM images of (A) etched Si pillars, (B) closeup image of pillars showing DRIE scallops and positively sloped resist, (C) after LPCVD poly-Si deposition and (D) higher magnification of sidewall profile after LPCVD deposition.
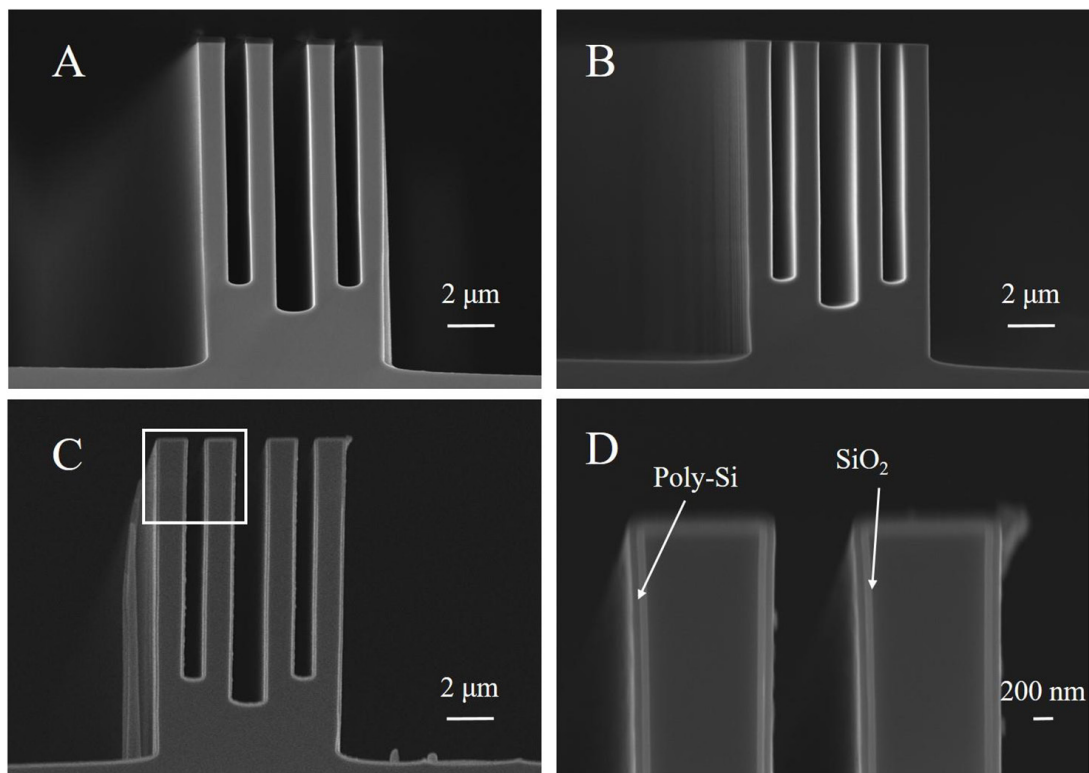

Figure 4. Demonstration of LPCVD poly-Si deposition with a SiO$_2$ layer for visualization purposes to differentiate deposited poly-Si layer from Si pillars. (A) Freshly DRIE etched sample as the start point, (B) dry oxidation of (A), (C) LPCVD poly-Si deposition of (B) and (D) higher magnification of (C).
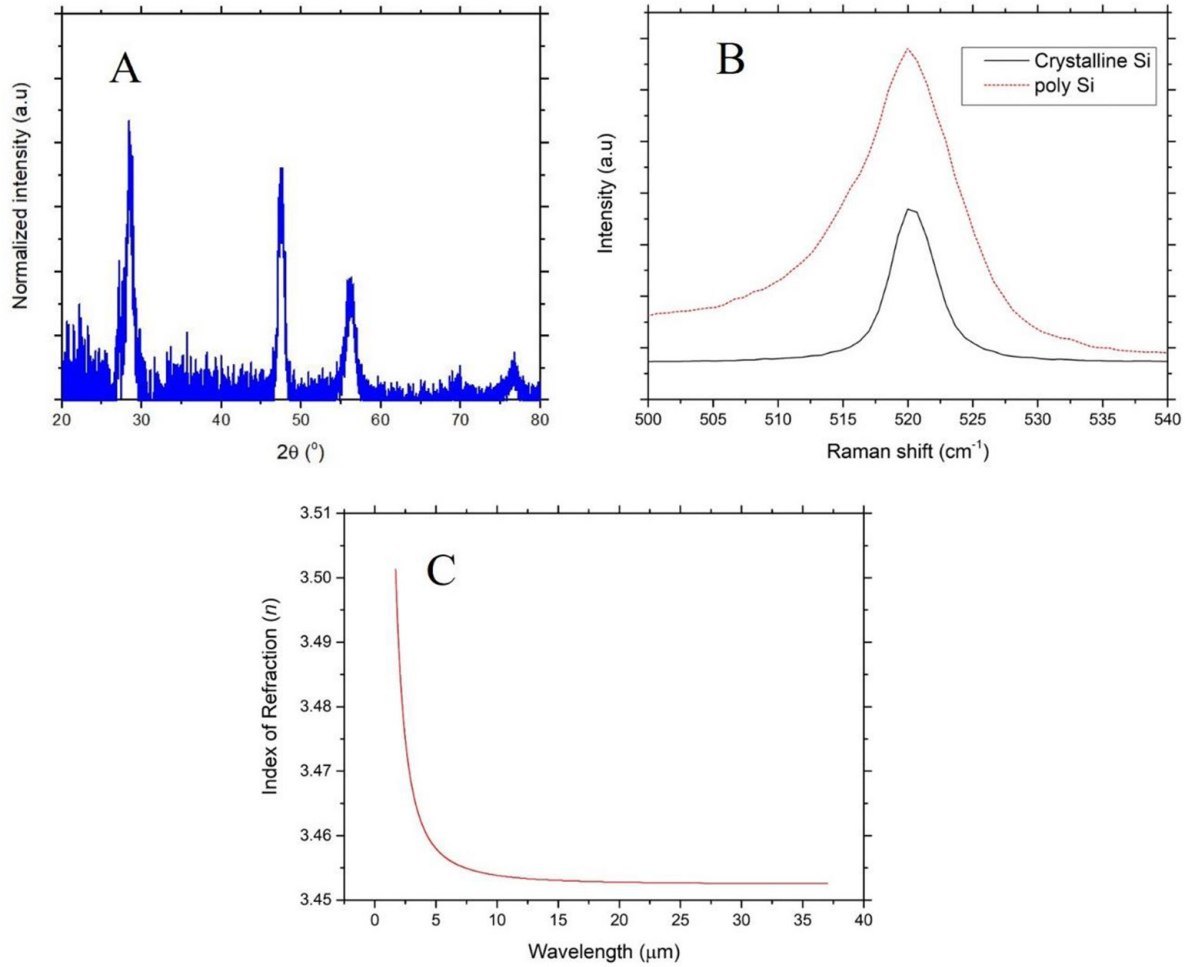
Figure 5. (A) XRD performed using detector-scan mode with theta at 1° for the elucidation of LPCVD deposited poly-Si with peaks corresponding to that of Si (28.5°, 47.4°, 56.2°, 69.4° and 76.8°) and SiO$_2$ (between 25.6° and 28.1°), (B) Raman spectroscopy for the elucidation of poly-Si microstructures and (C) LPCVD poly-Si refraction index determined using ellipsometry from 1.7–37.0 μm.

pillar. From the observation, the same thickness of poly-Si was deposited throughout the pillars regardless of the linespace width. Figure 4(D) is magnified from the boxed region as shown in figure 4(C). The thickness of the poly-Si layer was consistent with that on a piece of wafer monitor placed beside the sample during the LPCVD process.

The nature of the deposited poly-Si was further studied using XRD. XRD was performed on the wafer monitor using detector scan mode with theta being set to 1° as shown in figure 5(A). The diffraction peaks at 28.5°, 47.4°, 56.2°, 69.4° and 76.8° correspond to Si (1 1 1), (2 2 0), (3 1 1), (4 0 0) and (3 1 2), respectively. The deconvoluted peak located between 25.6° and 28.1° is attributed to the presence of SiO$_2$. The diffraction peaks matched those as described by JCPDS cards 00-027-1402 and 01-078-1256 for Si and SiO$_2$ respectively. The Scherrer formula was utilized to estimate the mean crystallite size of deposited poly-Si. By using the information gathered from the peak present at 47.4°, an approximated crystallite size of 10 nm was obtained by using equation (3). The results suggest that nanocrystalline Si was deposited on the surface

$$B\left(2\theta\right) = \frac{K\lambda}{L\cos\theta}. \tag{3}$$

Where B is the FWHM of the peak, K is the Scherrer constant taken to be 0.9, λ is the source wavelength, L is the crystallite size and θ is the measured peak angle. One main issue with the use of poly-Si is the presence of grain boundary which could potentially contribute to the propagation loss attributed to grain boundary scattering [24]. Such loss can be mitigated by increasing the LPCVD process temperature. Alternatively, the deposited poly-Si can be thermally annealed at temperature above 1000 °C to increase its grain size [25].

Deposited poly-Si assumed a similar peak position as crystalline Si at 520 cm^{-1} as shown in figure 5(B). The insignificant Raman shift results point to the fact that the deposited poly-Si had low residual stress when deposited at 625 °C [26]. Low-stress pillars are preferred to prevent structural deformation. As mentioned by Benrakkad *et al*, poly-Si has a higher Raman peak intensity as compared to crystalline Si [27]. The peak broadening suggests the presence of grains while the asymmetry of the poly-Si peak at 520 cm^{-1} revealed the
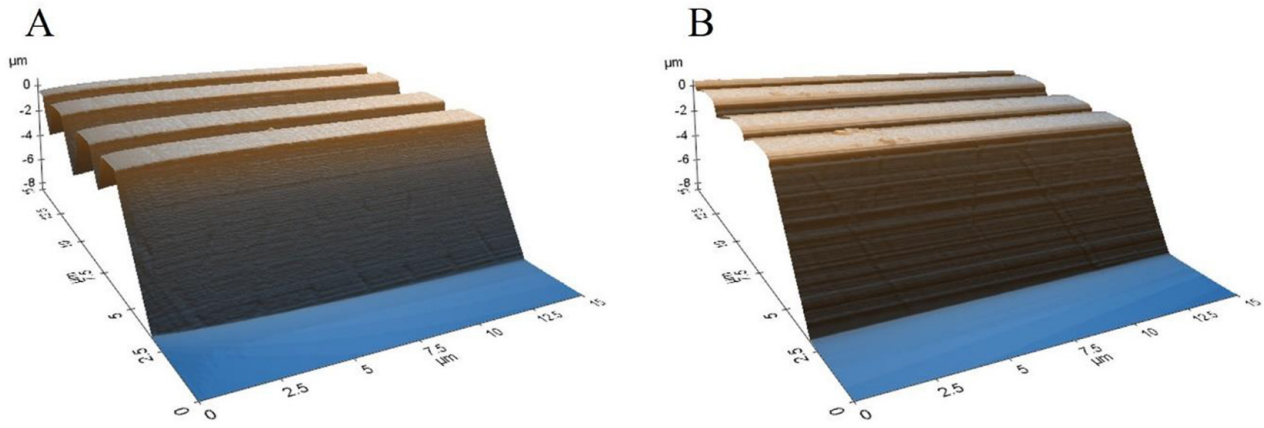
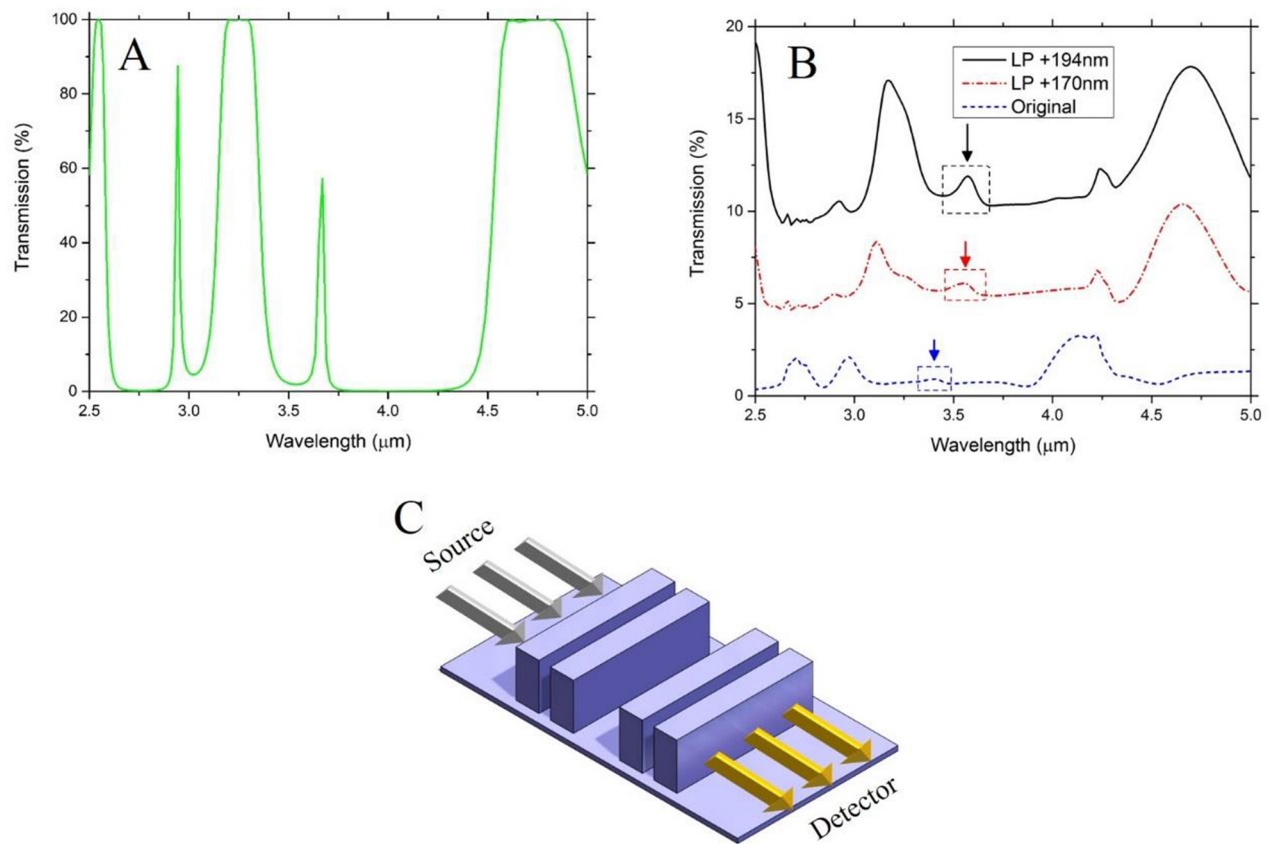**Figure 6.** AFM images showing sidewall topography of (A) before and (B) after LPCVD poly-Si deposition.

Figure 7. (A) Simulated bandpass and bandstop for DBR (Si and air of 1.45 μm and 1.00 μm) and cavity gap distance of 1.70 μm, (B) FTIR measured data for post etched as well as LPCVD poly-Si deposited samples with different amount of poly-Si deposited at 625 °C and (C) schematic diagram showing the working principle of a wavelength selective FPI.

nanocrystallinity nature of the sample, confirming the results obtained by XRD shown in figure 5(A) [28].

Measured optical constants of deposited LPCVD poly-Si is as illustrated in figure 5(C). Optical constants for both poly-Si and free-carrier properties of underlying Si were fitted to obtain best-fit curves. The acquired poly-Si refractive index (n) follows a decreasing trend while the extinction coefficient (k) is zero up to 37.0 μm. At 3.9 μm, $n_{poly-Si}$ and n_{Si} are 3.46 and 3.42, respectively [29]. Since the $n_{poly-Si}$ value is close to that of n_{Si}, $n_{poly-Si}$ could be approximated to n_{Si} for simplicity in all simulations. Amorphous Si and crystalline Si refractive

indices are well reported in the literature. To date, there have been no reports of experimentally measured poly-Si refractive index beyond 1.70 μm. Given the nature of poly-Si, its refractive index could be presumed to be between that of amorphous and crystalline Si. According to de Dood *et al*, 'Amorphous Si refractive index is around 0.3 higher than that of crystalline Si'. The authors purported that the difference in the refractive index is due to the difference in electronic band structure between amorphous and crystalline Si [30]. As the nature of poly-Si is between that of amorphous and crystalline Si, we can assume that the higher refractive index seen in poly-Si
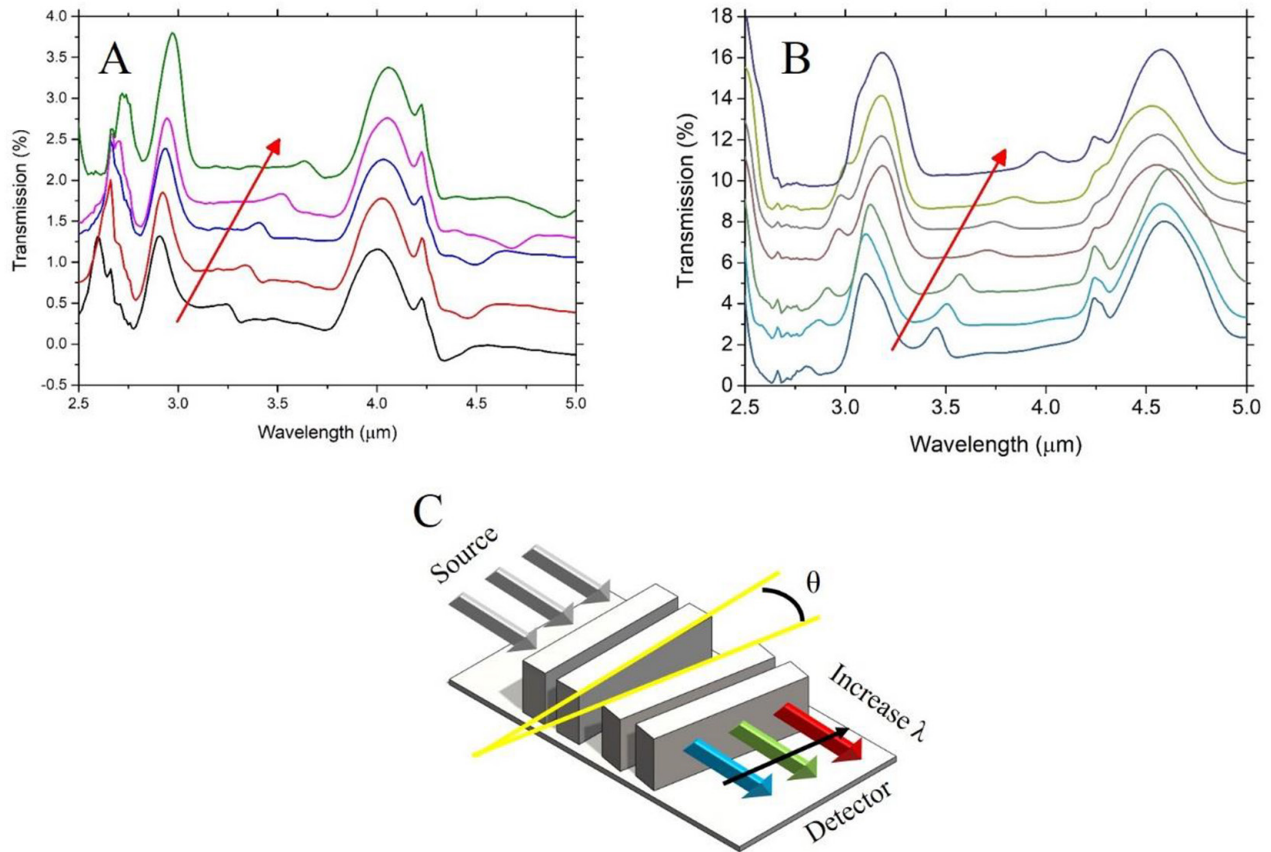
Figure 8. (A) As-fabricated LVOF with working range from 3.0–3.9 μm and (B) LVOF with 194 nm thick poly-Si showing improved passband intensity as well as red shifted transmission passband from 3.3–4.5 μm and (C) schematic illustration of LVOF working principle and selective wavelength transmitted along the length of the filter.

could also be due to slight variations in electronic band structure. Conducting a separate experiment and/or computational study to confirm the claim in the near future is suggested.

Vertical, non-destructive AFM was performed to elucidate the surface roughness (R_q) before and after poly-Si deposition of 194 nm as shown in figures 6(A) and (B) respectively. Sampling was performed using an AC160 cantilever tip, which is available from Park Systems. All samples were deep-etched using the Bosch process. The measured surface roughness, R_q, was approximately 12.0 nm. When poly-Si was deposited, the sidewall roughness (R_q) increased to 27.2 nm. The increase in roughness was likely attributed to the growth of nanocrystalline poly-Si and its associated microstructures [31]. Despite the rougher surface, it was shown in a later section that higher transmission was optically measured after compensation. Therefore, it could be inferred that even though surface roughness could contribute to propagation loss, it is most likely a secondary factor. Although not demonstrated in this work, the subsequent reduction in sidewall surface roughness could be carried out with repeated thermal oxidation and oxide etching in hydrogen fluoride [32].

With reference to figure 7(A), the intended passband was designed for 3.67 μm. However, the optical measurement performed on etched samples revealed a blue shift of the 'Original' passband as shown in figure 7(B) to 3.40 μm. The high loss in transmission passband could be a consequence of

an imperfect fabrication technique. As shown in figure 3(A), a total of about 200 nm of the Si pillars was etched away. The measured FWHM of the 'Original' line was about 80 nm. The working principle of an FPI is shown in figure 7(C) where the passband is selected by the DBR and the cavity distance.

As a proof of concept, two different poly-Si deposition thicknesses were demonstrated as shown in figure 7(B). The lines were plotted with a y-offset of 5%. When a total of 170 nm poly-Si (LP + 170 nm) was deposited, the passband shifted to 3.54 μm. In the event that 194 nm poly-Si (LP + 194 nm) was deposited, the passband was further red-shifted to 3.57 μm. For the latter, it could be observed that the bandstop peaks were located at approximately 2.90, 3.25, 4.75 μm in which they closely resembled that of simulated results. In all three cases, the FWHM remained unchanged suggesting that FWHM only depends on the verticality of pillars. Thus, this work indicates that the deposition of LPCVD poly-Si was highly conformal especially along the vertical height of the Si pillars. The distinct peak presented at 4.26 μm was due to the presence of atmospheric CO_2 in the laboratory. Prior to compensation, the passband has a peak transmission intensity of 0.20%. Despite rougher poly-Si coating on Si pillars, transmission signal intensity improved by approximately three-fold (0.57%) and seven-fold (1.35%) for LP +170 nm and LP + 194 nm, respectively. This is likely due to the consequence of recovering the designed linewidth and line spacing.

Signal attenuation, as observed in figure 7(B), could be attributed to the following reasons. It is plausible that optical loss was caused by the scattering of due to sidewall roughness induced by DRIE as well as imperfectly etched non-vertical vertical pillars [33]. Moreover, as the background reference of FTIR was performed in air, it does not account for the reflection at Si-air interfaces. Thus, the measured transmission was expected to be lower. With poly-Si compensation, transmission % should improve to that of the simulated intensity given the recovery of designed Si and air linewidth. However, underestimated experimental performance suggests imperfections of the fabricated poly-Si layer. This could be due to grain boundary scattering and absorption as a result of the presence of dangling bonds [34].

Subsequently, LVOFs were fabricated and characterized. During optical measurement, the mounted filter was scanned laterally by adjusting the microscope stage manually. The measured outcomes are shown in figures 8(A) and (B). The typical working principle of an LVOF is illustrated in figure 8(C). The as-fabricated LVOF as shown in figure 8(A) had a working range of 900 nm from about 3.0–3.9 μm. When 194 nm of poly-Si was deposited onto the pillars as shown in figure 8(B), the working range increased to 1200 nm. In addition, the working range also increased to 3.3–4.5 μm. This could be likely attributed to the effect of reducing fabrication error made possible by poly-Si compensation as well as the compensated LVOF achieving its designed linewidth and spacing. The effect of well-discussed broadening FWHM with increasing wavelength was observed. The band stops at approximately 2.90, 3.25 and 4.75 μm corresponded with that of the simulated result as shown in figure 7(A). This also suggests that an approximation using equation (1) could be utilized for the design of LVOF.

LPCVD deposited poly-Si was demonstrated to be the material of choice for linewidth compensation for Si substrates. While not shown in this work, overcompensated structures could be trimmed by repeating thermal oxidation—oxide etch in hydrogen fluoride. By coupling oxidation—oxide removal and LPCVD poly-Si deposition processes, one can gain absolute control over decreasing and increasing linewidth, respectively.

With this proposed technique, batch-to-batch variation induced during DRIE, an issue for foundry volume production, could be resolved. Future work concerning linewidth compensation for Si photonics applications should include the study of maximum compensation allowed by the proposed poly-Si deposition. It is also imperative to note if the LPCVD poly-Si deposition process is trench depth dependent. This warrants deeper trenches to be fabricated. Furthermore, the authors would like to propose that such a technique could be explored in other MEMS or MOEMS devices. Examples of use include compensation of material loss due to long-term operation for MEMS devices caused by friction. Such a technique illustrated could be explored to rectify imperfectly fabricated Si photonics and many other related applications. In particular, for the fabrication of narrowband optical filters, one can fine-tune the filter to target specific analyte spectral lines without resorting to the creation of various mask designs.

Conclusion

Many MEMS or MOEMS devices require the use of photoresist and DRIE to fabricate deep structures. One of the issues is that the positively sloped resist can cause the etched pillars linewidth to be less than the intended design during pattern transfer into the Si substrate. In order to overcome this problem, it becomes a requisite to perform mask design compensation. Yet, it does not resolve the issue of batch etching variation. Thus, an alternative to mask design compensation is proposed in this work. The authors proposed and showcased the concept of depositing LPCVD poly-Si on DRIE-ed samples to recover Si linewidth loss during etching. As-fabricated FPI samples were demonstrated to regain designed characteristics. This one-step process enables the deposition of a highly conformal poly-Si layer on etched pillars. Finally, the concept was applied to fabricate an LVOF with an initial working range from 3.0–3.9 μm. The transmission range red-shifted to 3.3–4.5 μm after poly-Si deposition. By coupling poly-Si deposition and oxidation—oxide etching processes, fine-tuning of structures could be achieved.

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