Pull-In Voltage and Fabrication Yield Analysis of All-Metal-Based Nanoelectromechanical Switches

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***Abstract*— We designed a one-mask process for all-molybdenum-based laterally actuated nanoelectromechanical switches. The damascene-like process is designed to ensure a smooth, high-aspect ratio, and metal-to-metal mechanical contact. Based on the statistical study of 800 devices, very high process yield can be achieved for fixed–fixed beam devices by selecting suitable device dimensions, i.e., the beam length versus beam width ratio should be <70 and the ratio of actuation gap to contact gap should be >1.5. Typical failure modes are also discussed. [2014-0391]**

***Index Terms*— Switches, nanoelectromechanical systems, electrostatic devices.**

I. Introduction

ELECTROSTATICALLY actuated micro/nano electromechanical system (M/NEMS) switches have been attracting attention for their excellent switching properties including zero-leakage current, abrupt switch behavior and potential to operate in high temperature [1]–[5]. These unique properties make NEMS switch a strong candidate for ultra-low power electronics and harsh environment integrated circuit (IC) [6]–[10].

On the other hand, it would be difficult for NEMS switches to entirely replace CMOS transistors in high performance ICs, since NEMS switches have lower a operating frequency due to their large mechanical delay. To avoid the low speed NEMS switches slowing down the circuit and fully utilize their zero leakage properties, several applications have been proposed for NEMS-CMOS integration, by using NEMS switches to replace speed insensitive elements in field programmable gate array [11]–[15], power gating [16]–[18] and static random access memory [19]–[21]. Studies indicate that introducing NEMS switches would largely reduce the power consumption of the whole NEMS-CMOS IC. To realize hybrid NEMS-CMOS circuit [22], [23], directly fabricating NEMS switches on top of CMOS layer would be a realistic and cost-effective technique. The semiconductor industry has developed air gap back end process [24] which is most suitable for the NEMS-CMOS hybrid circuit.

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The following requirements should be fulfilled to enforce NEMS-CMOS integration: i) The NEMS switches should be realized by a low temperature CMOS-compatible process for the ease of implementing the process in a modern CMOS foundry; ii) A simple process is desired; especially when it can leverage the existing metallization process; iii) The topography of the device should be small, to ensure the easy realization of devices with multiple layers stacking and wafer level encapsulation.

By far, most of NEMS switches are not suitable for the NEMS-CMOS integration. Many reports lack demonstration of repeatable on/off switch behavior [2], [6], [25], while a few reliable prototypes still need complicated processes to achieve robust structures. Yield of processes has not been addressed by recent studies [26]–[28]. All-metal based NEMS switches seem to be a reasonable choice to align with post-CMOS process. Our preliminary study [29] shows that all-metal based fixed-fixed beam NEMS switch has reliable performance even under accelerated high temperature measurement.

This work focuses on developing a robust, high process yield method for fabricating all-metal-based NEMS switch. It targets to achieve a single mask, CMOS compatible process for NEMS-CMOS integration applications as well as NEMS-only logic circuits. It also includes a basic method for NEMS switch designers to quickly identify the pull-in voltage and suitable device dimension. Device fabrication yield and typical failure modes are also discussed in the later section.

II. Design Consideration

In this study, laterally actuated switches are chosen because they can be fabricated with a single mask process, with all terminals formed in a single etching step (Fig. 1(a)). In comparison, vertically actuated mechanical switches need 4∼8 masks, multiple deposition and etching steps to assemble all terminals layer by layer. For three-dimensional integration, laterally actuated NEMS switches appear to have a much smaller topography, so that another layer of devices can be conveniently stacked on the existing device layer with a sacrificial layer and vias in between (Fig. 1(b)) [13], [30]–[34]. Since only one deposition step is involved in the laterally actuated switch fabrication, metallic material is most favorable for its low process temperature and low resistivity. As most of the device failures happen in the contact area, including welding, material transfer, delamination, and destruction [35], metal of high hardness and high melting point are commonly used, such as ruthenium [36]–[39], tungsten [40]–[42].

As a result, molybdenum, with high melting temperature of 2623°C and relatively high hardness, is selected as the

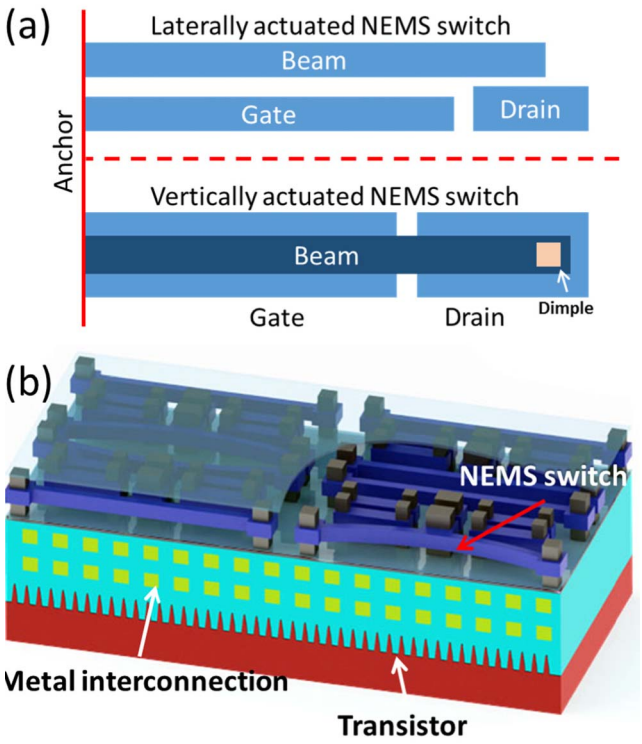

Fig. 1. (a) Top view of a laterally actuated NEMS switch and vertically actuated NEMS switch. (b) Schematic of building laterally actuated NEMS switches above CMOS.

structural material in this study. Among the high melting temperature metals, molybdenum has a low thermal expansion coefficient, and thus the mechanical deformation of the released structure would be less significant over a wide range of operation temperature. The processes for molybdenum deposition and dry etching are CMOS compatible.

The most critical step in the laterally actuated switches fabrication is the formation of actuation gap. A sub 100nm width is needed to obtain a suitable pull-in voltage. Further scaling down the device dimension requires an even smaller gap. Meanwhile, the etched sidewall has to be vertical and smooth in order to achieve larger contact surface area. Extremely clean surface is wanted, because contamination between contact surfaces could cause high contact resistance and localized heat flux fusing the contact. The existing metal etching process normally has a low aspect ratio and lacks a thorough cleaning method. Last but not the least, the metal thin film should be thick enough to limit the deformation within a reasonable level. To address these concerns, the fabrication process described in the next section using single Damascene process concept is able to provide the NEMS switches with a clean, smooth, high aspect ratio metallic contact surface. Both fixed-fixed beam and cantilever design have been fabricated with various device dimensions as shown in Fig. 2.

III. Fabrication Process

The process has been briefly introduced in [29], we would like to share some in-depth discussion and consideration. Unlike conventional process designed for laterally actuated

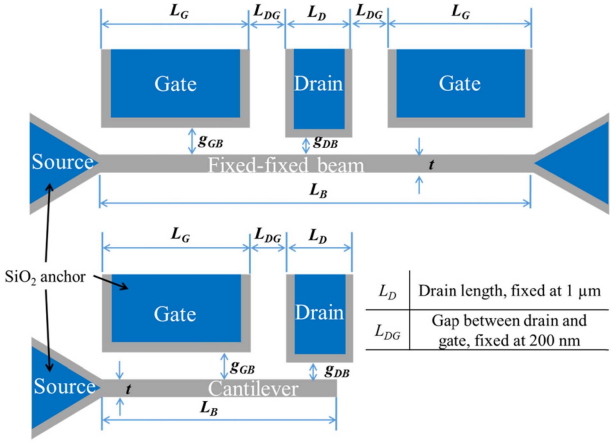

Fig. 2. Schematic drawing of a fixed-fixed beam switch and a cantilever switch.

NEMS switches (Fig. 3(a)), the fabrication process described below defines the active parts of the switches, by filling metal into a silicon dioxide mold. It starts from a Si wafer with 1 μm silicon dioxide layer. Deep UV photolithography using 200 nm critical dimension mask defines the oxide features. Then the oxide layer is etched for 400 nm with reactive-ion etching (RIE) (Fig. 3 (b)). As a result, 600 nm oxide is left on the bottom of the oxide trench for insulation purpose. At this step, an oxide fin is formed, which serves as a mold for metal structures as well as the sacrificial layer. After photoresist strip, the surface is cleaned with Piranha solution, and then wet etching is performed in diluted hydrofluoric acid (DHF) to reduce the oxide fin thickness (Fig. 3(c)). Then 300 nm molybdenum is sputtered (Fig. 3(d)), followed by 500 nm high-density plasma chemical vapor deposition (HDP CVD) SiO_2 to fill all the trenches (Fig. 3(e)). A SiO_2 chemical mechanical polishing (CMP) process is performed to expose the top molybdenum layer. The remained oxide is used to protect the structural layer beneath (Fig. 3(f)). Afterward, 300 nm molybdenum etching is done by RIE, to ensure the exposed top molybdenum layer is removed and only bottom molybdenum structural layer is left (Fig. 3(g)). Thus, the actuation gap and insulation between terminals are formed at the same time. The devices are finally released by vapor hydrofluoric acid (VHF) system (Fig. 3(h)). All processes are under 400 °C.

At the DHF etching step, when minimum dimension is used for both gap and beam width, decreased oxide fin thickness reduces the pull-in voltage. Meanwhile, adding extra layer of SiO_2 on the sidewall achieves a similar effect. However, reducing the oxide fin thickness seems to be a better choice, as the metal beam width is increased at the same time. Wider beam provides better thermal conductivity to quickly conduct the heat generated in the contact area. It has a higher resonant frequency and switching speed. It is also more resistant to the beam to gate pull-in failure.

Scanning electron microscope (SEM) photos are taken during critical fabrication steps. Fig. 4(a) shows the oxide fin after wet etching with 100 nm thickness and straight sidewall profile. Fig. 4(b) shows the fully-covered oxide layer and

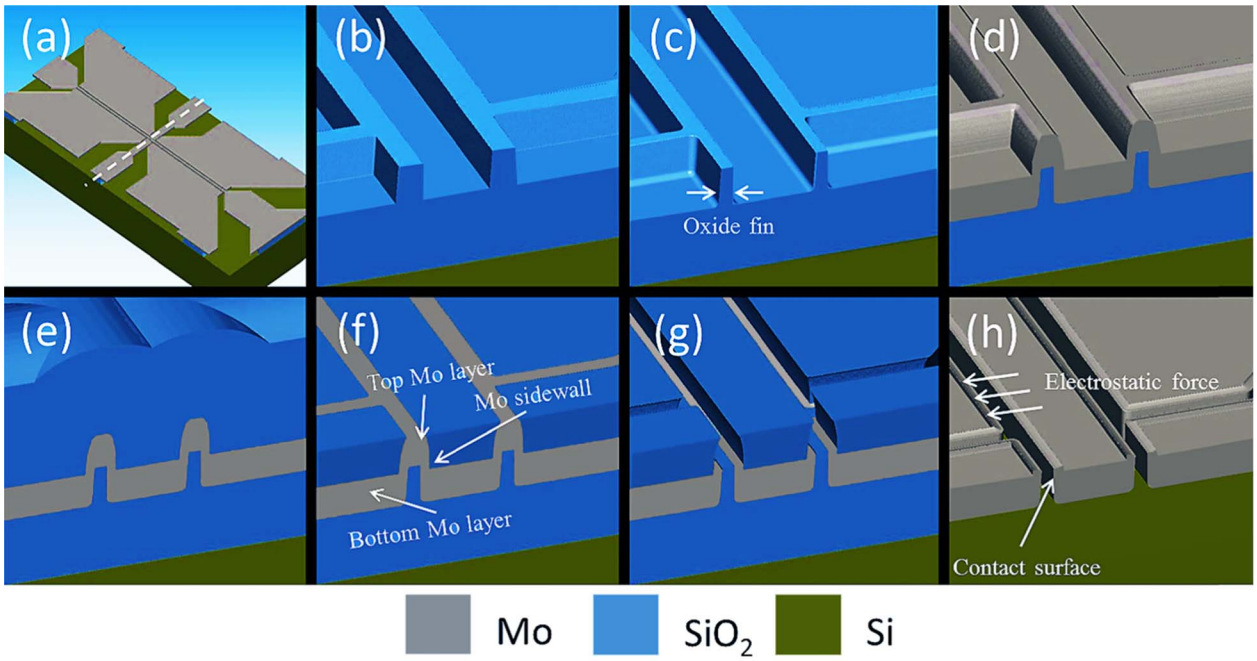

Fig. 3. (a) The white dash line indicates the cross-section used in the following figures (b) SiO_2 RIE forming the trench (c) Wet etch reducing the oxide fin thickness (d) 300nm molybdenum PVD (e) 500nm HDP CVD SiO_2 (f) SiO_2 CMP (g) molybdenum RIE (h) VHF release.

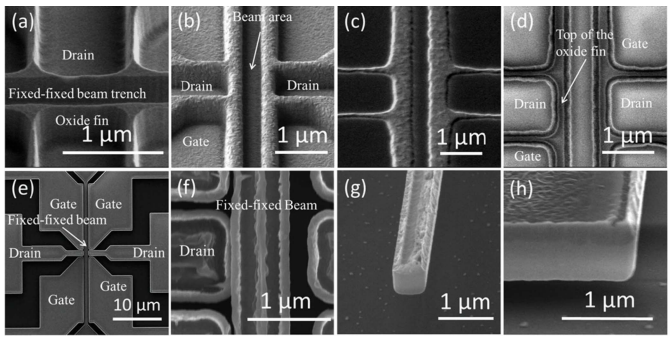

Fig. 4. SEM photos of devices near the contact region after (a) wet etch, (b) Mo deposition, (c) oxide CMP and (d) Mo RIE. (e) Whole device after release. (f) Fixed-fixed beam pull-in by electron charging. (g) Test structure of a single beam. (h) Test structure of contact surface.

large grains on the surface after molybdenum PVD. Fig. 4(c) shows molybdenum on top of the oxide fin can be successfully exposed after the oxide CMP step across the whole wafer. Fig. 4(d) shows the top molybdenum layer is etched away, and the upper edge of the oxide fin is exposed. Fig. 4(e) shows a released fixed-fixed beam device. Fig. 4(f) shows the zoomed-in view of the contact area, where the beam is attracted to the drain terminal by accumulated electron charges. The cantilever test structure (Fig. 4(g)) shows the molybdenum sidewall on the edges of the bottom molybdenum layer is almost etched away. The smooth molybdenum sidewall profile is shown in Fig. 4(h), where no visible grain can be found.

The differences between the proposed process above and conventional process are shown in table I. SiO_2 insulation layer and molybdenum structural layer are used in both cases.

TABLE I
PROCESS DIFFERENCES BETWEEN THIS WORK AND CONVENTIONAL WORK

Item	This work	Conventional process
Process Sequence	SiO_2 CVD➔SiO_2 Etching ➔Mo PVD➔SiO_2 CVD ➔SiO_2 CMP➔Mo Etching ➔VHF	SiO_2 CVD➔ Mo PVD➔Mo Etching ➔VHF

Although a few more steps are added, the proposed process shifts the formation of contact surface from molybdenum etching to deposition. The contact surface is not exposed until VHF release, which ensures etching residual do not contaminate the surface. The back end process in CMOS foundry could adapt this process easily with conventional dual-Damascene process.

IV. ELECTRICAL MEASUREMENT OF A TYPICAL DEVICE

A typical fixed-fixed beam device is picked first to verify the electrical performance. The measurement is conducted in a vacuum wafer probing system (Cascade Microtech, PMV200, vacuum level: 5.4E-6 mbar) using a semiconductor parameter analyzer (Agilent Technology, B1500A). It is first tested for double side I-V sweep with 500 nA current compliance. General NEMS switch behaviors, including abrupt switching, zero off-state current and hysteresis behavior can be found in Fig. 5(a). Afterward, higher current in the drain terminal is tested, and an exceptionally high current of 1 mA is applied with a 5s interval. The device shows a stable electrical performance in Fig. 5(b) with an on/off ratio of 10^8.

The contact resistance of this device is also measured with 0.1V constant voltage at the drain terminal. The small

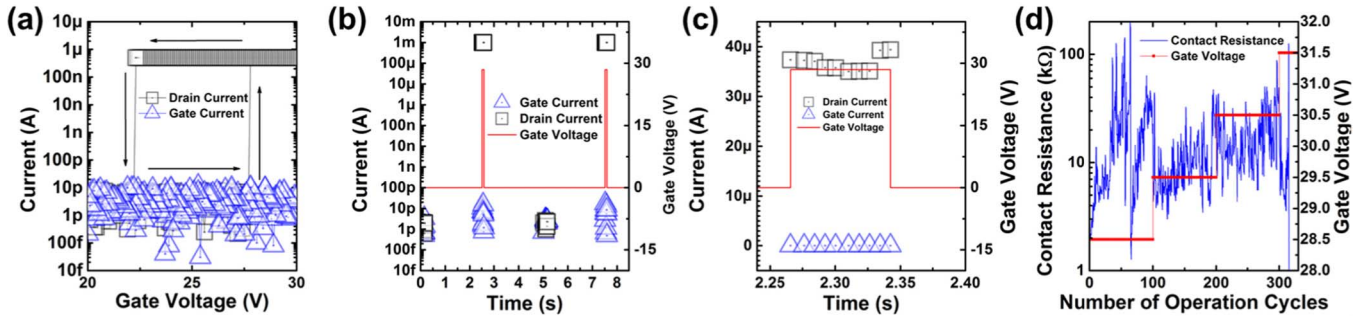

Fig. 5. Electrical tests for a fixed-fixed beam device with dimension of $L_B = 28$ μm, $t = 700$ nm and $g_{GB} = 150$ nm (a) I-V sweep with 500 nA current compliance. (b) Cycling test with 1 mA current applied on drain terminal. (c) Cycling test to obtain contact resistance. (d) Contact resistance change over the cycling test.

drain voltage value is set to prevent the excessive current to damage the contact. The current compliance is removed from this cycling test. Fig. 5(c) shows that in the initial cycle, the contact resistance is around 2.5 kΩ, indicating a good metal to metal contact. Fig. 5(d) reflects the contact resistance measured at every cycle. For the first 100 cycles, the gate voltage is set to be 28.5 V, the same as the measurement in Fig. 5(b) and (c). The contact resistance gradually increases and suddenly drops in the 56th cycle, and again the resistance increases afterward. Then the gate voltage is increased to 29.5V and 30.5V. The contact resistance has a drop after voltage increases, and stabilizes at 5∼20 kΩ. After increasing the voltage to 31.5V, the beam collapses on the gate terminal, causing the gate to beam shortage which cannot be recovered afterward. The measurement indicates that a higher gate voltage helps to stabilize the contact resistance, but further improvement should be done by proper surface coating [43]–[45]. A long time accelerated reliability measurement can be found in [29]. A 28 μm long device is cycled for 28 hours under a 300°C environment without obvious performance degradation.

V. Statistical Study on Pull-In Voltage and Yeild

After single device study, statistical measurement of pull-in voltage and process yield have been carried by measuring 800 devices, which includes 500 fixed-fixed beam NEMS switches (50 different dimensions) and 300 cantilever beam switches (30 different dimensions). These 800 devices are picked from 5 different positions across the same wafer. Every chip contains two devices with identical dimension. Only two most important factors, beam length and beam thickness vary, while other parameters are fixed. All parameter combinations shown in table II are studied. Furthermore, for the fixed-fixed beam, two addition parameters, the actuation gap, g_{GB}, and the contact gap, g_{DB}, are also studied with two combinations.

Before electrical measurement, analytical solution and finite element modeling are performed to estimate the pull-in voltage for each dimension. With simple parallel-plate model, pull-in voltage of NEMS switch in vacuum is:

$$V_{pi} = \sqrt{\frac{8k_{eff}g_{GB}^3}{27\varepsilon_0 L_B w}} \tag{1}$$

Where w is the thickness of the beam, ε_0 is the permittivity of vacuum, k_{eff} is the effective spring constant of the beam,

TABLE II
Design Parameter

	Quantity	Design Value
Fixed-fixed beam	Beam length, L_B	28 μm, 32 μm, 40 μm, 60 μm, 100 μm
	Beam width, t	300 nm, 400 nm, 500 nm, 600 nm, 700 nm
	Gap, (g_{GB}, g_{DB})	(150 nm,100 nm), (200 nm,150 nm)
cantilever	Beam length, L_B	12 μm, 14 μm, 16 μm, 20 μm, 30 μm, 50 μm
	Beam width, t	300 nm, 400 nm, 500 nm, 600 nm, 700 nm
	Gap, (g_{DB}, g_{GB})	(150 nm,100 nm)

which is related to beam type and the electrostatic force distribution along the beam. For a more accurate k_{eff}, we consider the drain voltage is normally much smaller than the gate voltage, with no electrostatics force from drain terminal contributed to the pull-in. For fixed-fixed beam cases, the electrostatic force is missing in the middle of the beam. Thereby, the effective spring constant of the fixed-fixed beam is given by:

$$k_{eff} = \frac{4Ewt^3}{L_G^2(L_B - L_G)} \tag{2}$$

Where E is the young's modulus of molybdenum.

The pull-in voltage of the fixed-fixed beam is given by:

$$V_{pi} = \sqrt{\frac{32Et^3g_{GB}^3}{27\varepsilon_0 L_G^2 L_B(L_B - L_G)}} \tag{3}$$

Similarly, for cantilever case, we consider no electrostatic force at the tip of the beam:

$$k_{eff} = \frac{2Ewt^3}{L_G^2(4L_B - L_G)} \tag{4}$$

The pull-in voltage is given by:

$$V_{pi} = \sqrt{\frac{16Et^3g_{GB}^3}{27\varepsilon_0 L_G^2 L_B(4L_B - L_G)}} \tag{5}$$

Notice the structure layer thickness has been cancelled during the calculation, therefore it does not have an impact on the pull-in voltage in this model. There are a lot of assumptions for the parallel-plate model: a linear spring constant of the beam,

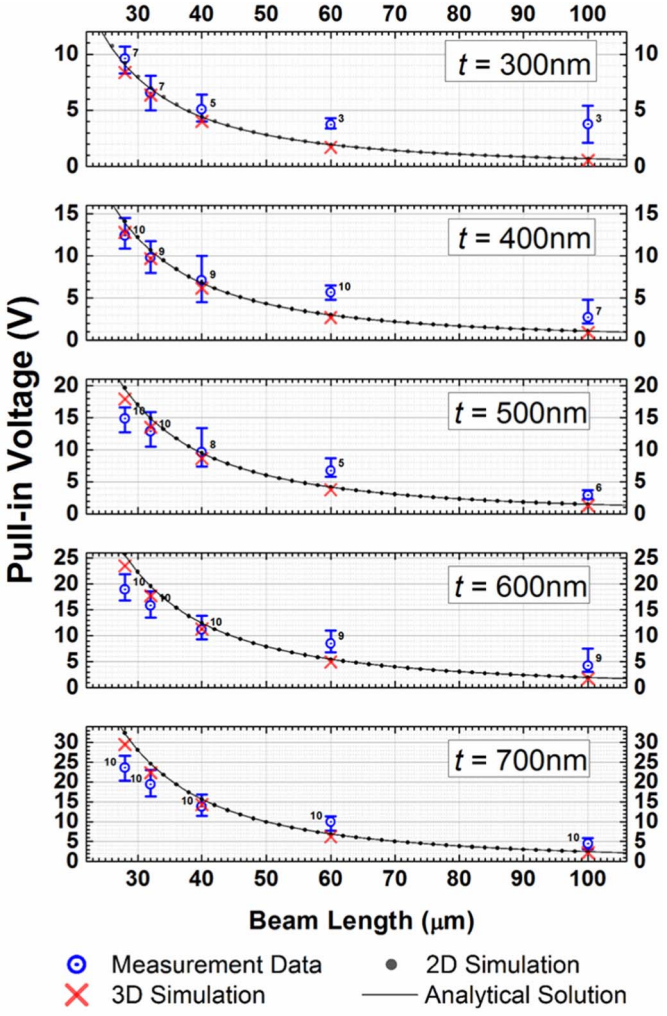

Fig. 6. Pull-in voltage summary of fixed-fixed beam devices with $g_{GB} = 150\ nm$, and $g_{DB} = 100\ nm$, with beam length L_B, beam width t varies.

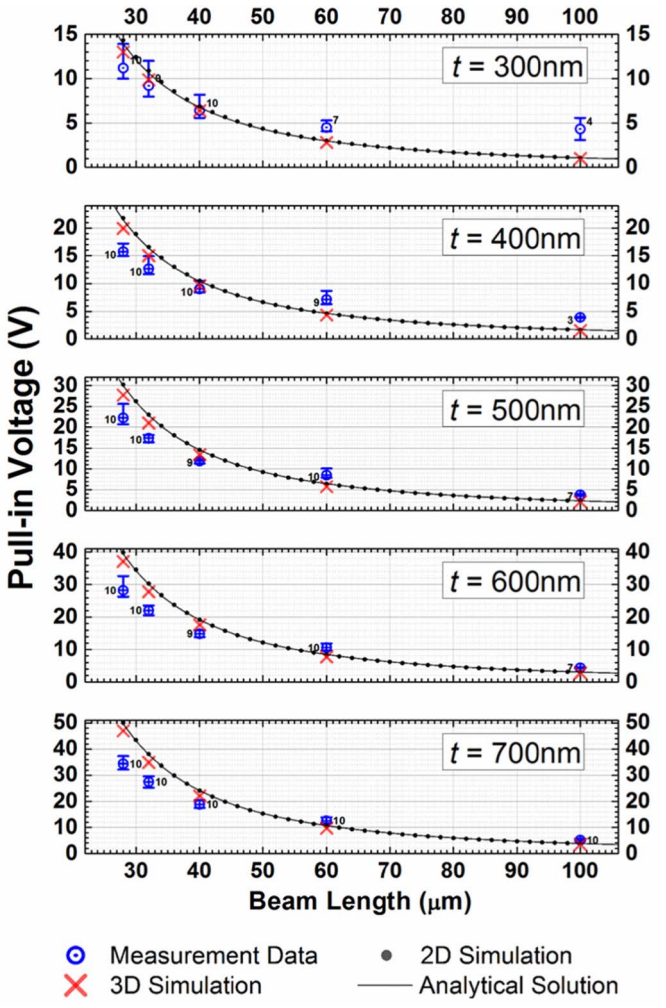

Fig. 7. Pull-in voltage summary of fixed-fixed beam devices with $g_{GB} = 200\ nm$, and $g_{DB} = 150\ nm$, with beam length L_B, beam width t varies.

a piston-like motion where pull-in always occurs when deformation reaches one-third of the actuation gap, no fringing field taken into account. 2D and 3D simulations are performed for higher accuracy, using COMSOL Multiphysics tool [46]. The 2D model covers a very wide range of dimension, and we only did 3D simulations of the dimensions shown in Table II. The simulation sweeps the voltage from a smaller guessed value until convergence failure near the pull-in, and then this voltage is recorded as pull-in voltage. The simulation generally takes quite a lot computational cost: one 2D simulation takes a few minutes, while 3D simulation needs tens of minutes using a state-of-art workstation.

The simulation results have been plotted in Fig. 6-8. Where Fig 6 is fixed-fixed beam device with g_{DB}=100 nm, g_{GB}=150 nm. Fig 7 is also fixed-fixed beam device, but with g_{DB}=150 nm, g_{GB}=200 nm, Fig 8 is the cantilever device with g_{DB}=100 nm, g_{GB}=150 nm. The 3D simulation results are typically 10% lower than the 2D simulation, which is most likely caused by the fringing field out-of-plane. Although so many assumptions are applied to the analytical solution, it appears that by simply adding a constant coefficient to equation (3) and (5), the analytical solution would fit the 2D simulation very well.

For fixed-fixed beam:

$$V_{pi} = a_{ff}\sqrt{\frac{32Et^3g_{GB}^3}{27\varepsilon_0 L_G^2 L_B(L_B - L_G)}} \tag{6}$$

For cantilever beam:

$$V_{pi} = a_c\sqrt{\frac{16Et^3g_{GB}^3}{27\varepsilon_0 L_G^2 L_B(4L_B - L_G)}} \tag{7}$$

By assigning $a_{ff} = 1.26$ and $a_c = 1.4$, the deviation between analytical solution and 2D simulation is only ±2% for fixed-fixed beam and ±4.5% for cantilever across the whole simulation range. For 3D simulation cases, assigning $a_{ff} = 1.2$ and $a_c = 1.3$, the deviation still reaches 10% in some cases. The accuracy of the analytical model is higher when L_B/t is smaller than 70, with ±4% for fixed-fixed beam and ±5% for cantilevers. Although the equation is constrained to a limited range, it is still acceptable as very high beam length to width ratio is not desired in actual design, which will be discussed later.

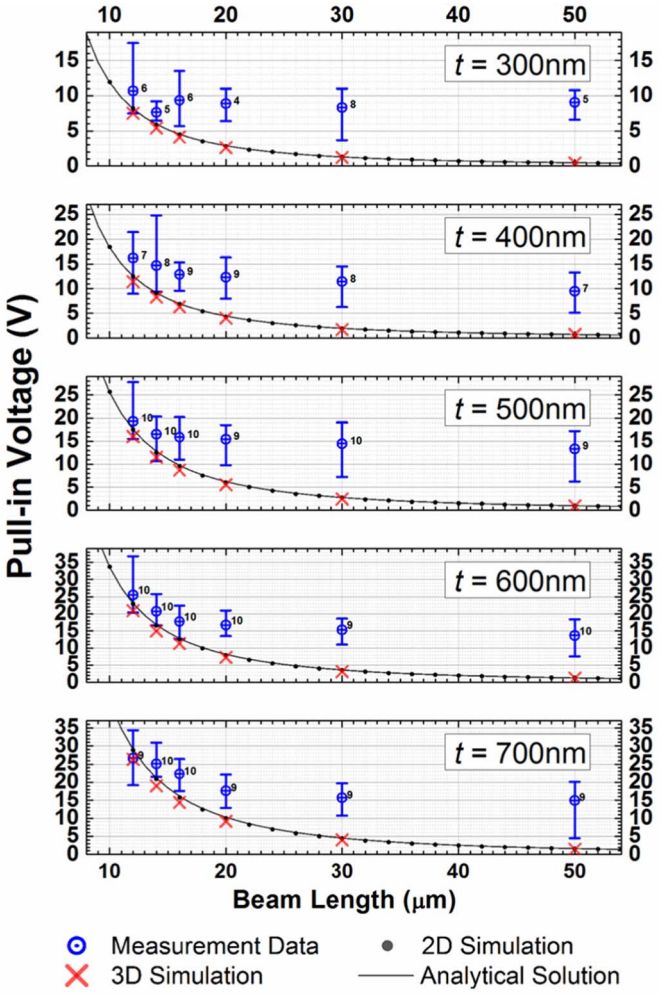

Fig. 8. Pull-in voltage summary of cantilever beam devices with $g_{GB} = 150\ nm$, and $g_{DB} = 100\ nm$, with beam length L_B, beam width t varies.

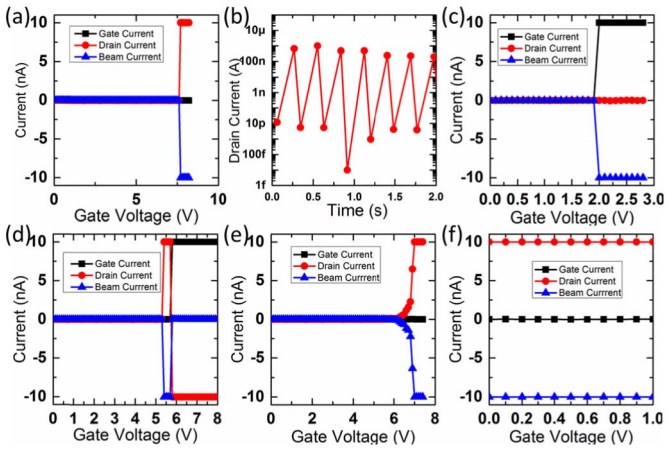

Fig. 9. (a) I-V curve of a repeatable device (b) cycling measurement of a repeatable device. (c) I-V curve of a gate to beam pull-in device. (d) I-V curve of a device to secondary pull-in. (e) First round I-V curve of a device with stiction (f) Second round I-V curve of a device with stiction.

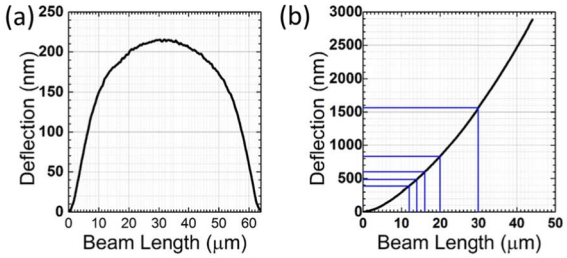

Fig. 10. (a) beam deflection of a 60 μm fixed-fixed beam. (b) beam deflection of a 50 μm cantilever.

With the prediction of the pull-in voltage, 800 devices are measured individually. The procedures are as follows: an I-V sweep starts from 0V with 0.1V step. 10 nA compliance is given to each terminal. Current from every terminal is monitored. Once pull-in phenomenon is observed, the I-V sweep would be terminated manually, and typically the device would be overdriven for 1V. Based on the measurement, we can classify the 800 measurements into 6 different categories below:

i. Repeatable devices: after the I-V sweep, a repeatable device shows beam current and drain current in the opposite direction. The gate current keeps at noise level as shown in Fig. 9(a). A quick cycling test (for around 100 cycles) shown in Fig. 9(b) verifies the repeatability. **ii.** Gate to beam pull-in: in I-V sweep, the gate current raises at the same time with the beam current or drain current as shown in Fig. 9(c), no cycling behavior can be observed in these devices. **iii.** Secondary pull-in: in the I-V sweep, the devices behave like the repeatable devices at first, but they quickly show the gate to beam pull-in right after the first pull-in as shown in Fig. 9(d). **iv.** Stiction: in I-V sweep, the signal is identical to the repeatable devices shown in Fig. 9(e). But in the following cycling measurement and I-V sweep as shown in Fig. 9(f), the devices have constant current between drain and beam even with 0V gate voltage applied. **v.** Short circuit: in I-V sweep, the drain current and beam current appear from the beginning of the sweep. **vi.** No signal: even after very large voltage overdrive, there is no current observed in any of the terminals.

Detailed causes of the failure will be discussed later. We focus on the pull-in voltage analysis first. In the above 6 cases, pull-in voltage can be obtained from case 1 to case 4. All pull-in voltage data have been plotted in Fig 6∼8, the number besides the measurement data show the quantity of the data.

Generally the measured pull-in voltages for fixed-fixed beam NEMS switches are smaller than simulation when beam length is smaller than 60 μm. In Fig 4(f), (g) and (h), an extra sidewall exists on every edge, which will induce an extra electrostatic force. On the other hand, when the beam length is larger than 60 μm, the pull-in voltage is much higher than expected. The test structure is checked under a holographic microscope (Lyncee Tec, DHM-R2200). For a 60 μm fixed-fixed beam, the maximum deflection in the middle is about 200 nm as shown in Fig. 10(a), therefore, the effective capacitance between gate terminal and beam terminal is much smaller.

For cantilever case, the problem becomes severe, as the test structure has a deflection of more than 300 nm at the point,

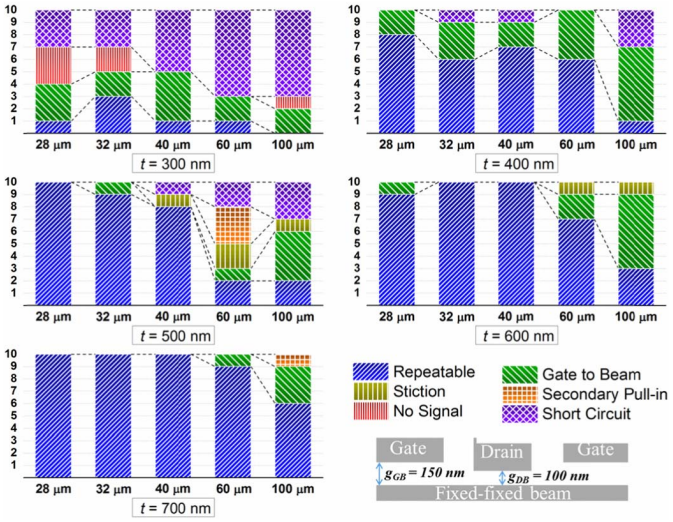

Fig. 11. Failure analysis of fixed-fixed beam devices with $g_{GB} = 150\ nm$, and $g_{DB} = 100\ nm$, with beam length L_B*(x-axis)*, beam width t varies. Number on y-axis indicate the count of different failure mode.

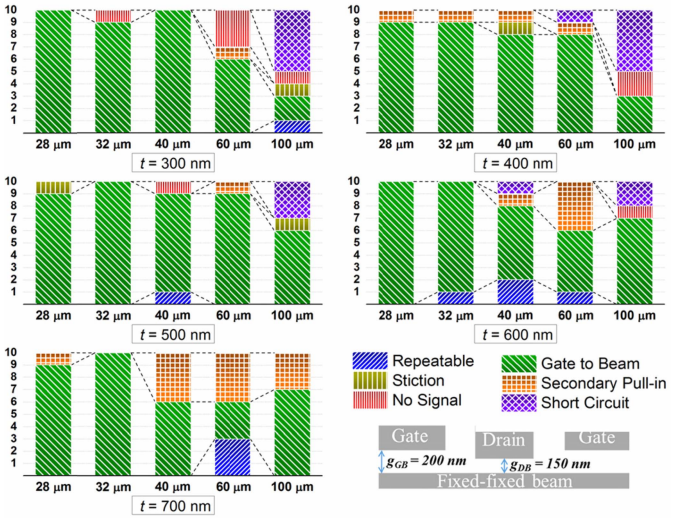

Fig. 12. Failure analysis of fixed-fixed beam devices with $g_{GB} = 200\ nm$ and $g_{DB} = 150\ nm$, with beam length L_B*(x-axis)*, beam width t varies. Number on y-axis indicate the count of different failure mode.

12 μm from the anchor, as shown in Fig. 10(b). As a result, only the first 12 μm near the anchor is effectively used for electrostatic actuation, and thus the mean value of the pull-in voltage does not decrease when the beam length increases from 12 μm to 50 μm. The pull-in voltages cover quite a wide range as the beam deflection varies across different positions of the wafer. We do observe that some devices have drain to beam contact even when the beam length is very long, which indicates in some area the bending is much smaller.

The deflection is induced by the stress gradient of the film deposited. We found no uniform control effect on the deflection is achieved even after thermal annealing, excimer laser annealing and Ar plasma treating. Nonetheless, if we can maintain the film thickness and keep scaling down all the other dimensions, the deformation can be confined to an acceptable level. Fixed-fixed beam with less than 40 μm beam length is preferable. For cantilever, the length should be smaller than 3 μm when targeting to achieve tip bending of less than 50 nm.

Next, we investigate the failure mode and process yield for different dimensions. Fig. 11∼13 show the count of different failure modes referring to the devices from Fig. 6∼8. For the above mentioned failure modes, it is difficult to confirm them in the SEM directly, as a beam to gate shortage normally leads to device melting.

In Fig. 11, the devices generally show very good repeatability with the beam width of t >500 nm and beam length of L_B < 40 μm. All 60 devices fabricated in the six groups show good repeatability and it indicates all groups have a perfect process yield. Overall, the predominant failure mode is the gate to beam pull-in, in which the beam cannot withstand the excessive electrostatic force and collapses on the gate terminal, after the beam touches the drain. Meanwhile, the secondary pull-in effect can be treated as a special case of gate to beam pull-in, as after a successful drain to beam touch, a small extra voltage makes the beam collapse on the gate. A few stiction cases can also be observed when the beam is too long, when the elastic force is not high enough to detach the beam

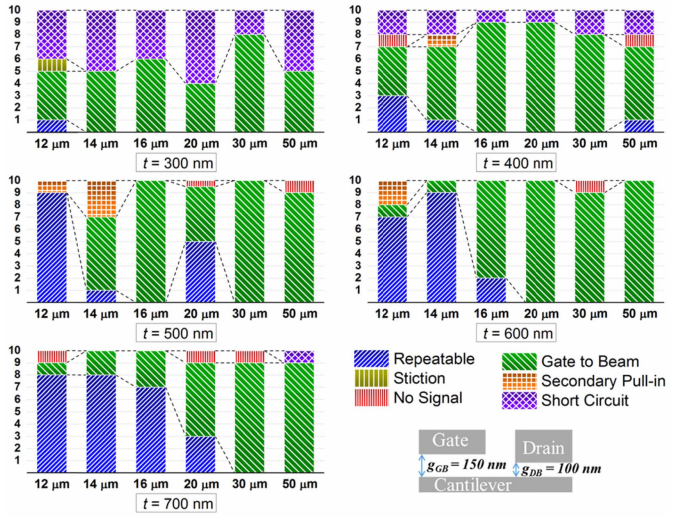

Fig. 13. Failure analysis of cantilever beam devices with $g_{GB} = 150\ nm$, and $g_{DB} = 100\ nm$, with beam length L_B*(x-axis)*, beam width t varies. Number on y-axis indicate the count of different failure mode.

from the drain terminal. The stiction mode is good for non-volatile memory application, but we fail to observe consistent stiction phenomena in all switches of certain dimensions, indicating that the van de Waals force on the contact surface varies from device to device. Thus, a wider drain terminal should be used for non-volatile memory devices.

Another major failure mode in this group is short circuit, it is understandable that very long and thin beams will touch the other terminal when the stress is high. However, the 300 nm wide beam group has a lot of short circuit devices. The main reason is that the etching step between Fig 3(f) and Fig 3(g) cannot fully etch away unwanted molybdenum, because the lithography condition is a bit different in the case of 100nm wide gap and 300 nm wide beam. This problem can be easily avoided by adding etching time. In logic circuit applications where the devices have similar gap and beam width.

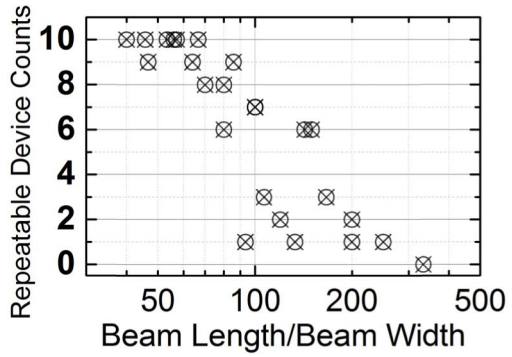

Fig. 14. Counts of repeatable device versus beam length to width ratio.

The similar reason, why some devices in that group have no signal when the gap opens on the actuation side, is that the beam is fixed on the other side caused by incomplete etching.

Most failures are closely related to the stiffness of the beam, the effective spring constant is antiproportional to (L_B/t) ^3. The process yield drops quickly with L_B/t >70 as shown in Fig. 14. As mentioned, in the fabrication process after the oxide mold is prepared, decreasing or increasing the oxide fin thickness has the similar effect on reducing the pull-in voltage. So reducing the oxide fin thickness is more favorable as it will also decrease the beam length to width ratio and improve the device yield as shown above.

For fixed-fixed beam with $g_{GB} = 200\ nm$ and $g_{DB} = 150\ nm$ shown in Fig 12, the dominant failure mode is the gate to beam pull-in. Compared to the previous group, all the dimensions are the same except for the gap width. The actuation gap to the contact gap ratio, $g_{GB}/g_{DB,}$ *is only* 1.33, where the previous group has a ratio of 1.5. The g_{GB}/g_{DB} ratio determine how close between the beam and the gate terminal after pulling-in comparing to the whole actuation gap. A low g_{GB} *to* g_{DB} ratio means the beam is closer to the gate terminal and more likely to collapse. Therefore, the difference between actuation gap and contact gap is a very sensitive factor for device yield, and maintaining a 1.5 ratio is a reasonable requirement.

Lastly, the cantilever failure modes are shown in Fig. 13. From previous discussion on pull-in voltage of the cantilever (Fig. 8), they suffer severe bending and the curvature varies from device to device. In the statistical measurement, most devices experience a direct beam to gate touch.

VI. Conclusion

In conclusion, we have reported all-molybdenum based NEMS switches fabricated by a one mask Damascene-like process. The low temperature process provides metal-based laterally actuated NEMS switches of 100 nm wide gap with smooth contact surface. A comprehensive statistical study of 800 fabricated devices lead to guidelines for high-yield NEMS switch design. Important factors of laterally actuated NEMS switch design are summarized below. Firstly, the deformation of the metal film needs to be carefully considered. Lack of method to eliminate the stress gradient, the only effective way is to maintain the metal film thickness and reduce the beam length simultaneously. For 300nm thick molybdenum film, maximum length of fixed-fixed beam and cantilever is 40 μm and 3 μm respectively. For certain critical dimension and pull-in voltage, a low beam length to width ratio is preferable to obtain a very high process yield. Actuation gap to contact gap ratio is also critical and should be no smaller than 1.5.

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