Fabrication and Characterization of a Vacuum Encapsulated Curved Beam Switch for Harsh Environment Application

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***Abstract*— A vacuum-encapsulated silicon switch with a curved electrode is characterized for operation in harsh environments. An ultraclean vacuum encapsulation process (episeal) seals the switch after release, providing a pristine operating environment for switching operations. In these devices, the curved beam of the actuator enhances the overdrive voltage tolerance to be more than 100 V. The ON/OFF cycle tests were carried out up to 10^5 cycles at room temperature, and at least 10^4 cycles under an elevated temperature of 300 °C. Throughout the 300 °C tests, an average contact resistance of ∼28 kΩ is measured, demonstrating the stability of the contact. Finally, high speed pulse *I–V* monitoring unit was used to observe 13-μs switching speed. [2013-0361]**

***Index Terms*— Rugged electronics, microelectromechanical systems (MEMS), electrostatic switch, relay, switch.**

I. Introduction

MICROELECTROMECHANICAL SYSTEMS (MEMS) electrostatic switches have been demonstrated and have potential to offer several unique features, such as near-infinite sub-threshold slope, near zero leakage and the potential for operation in harsh environment [1]–[3]. These features are due to the nature of micromechanical relays, where the static power dissipation is close to zero. Such characteristics make capacitive relays exceptionally efficient for power gating or ruggedized electronics applications [4]–[6]. Despite the potential for high energy efficiency and outstanding electrical characteristics, MEMS switches have yet to impact significant applications compared to existing state-of-the-art CMOS switch technology. However, MEMS switches have shown promising capability in CMOS-MEMS hybrid memory circuits and also standalone ruggedized logic operation in harsh environments where the requirements for these applications are beyond CMOS's physical limits [7]–[10]. While MEMS switches have demonstrated the capability of CMOS logic operation and non-volatile memory [11]–[14], some undesired properties such as secondary pull-in prevent or degrade the performance of MEMS switches [15]–[17]. The phenomenon of secondary pull-in is illustrated in Fig. 1. For cantilever and doubled-clamped beam designs, secondary pull-in can occur when the gate voltage is overdriven, and the excessive electrostatic force causes the beam to contact the gate, resulting in a short circuit and device failure. This may also happen during gate voltage spikes. Some reported MEMS switches implement a layer of dielectric insulation such as alumina (Al_2O_3) or silicon dioxide (SiO_2), between the gate and the actuation beam to prevent secondary pull-in and catastrophic short circuits [18]–[20]. These dielectric layers can prevent device failure, but also seriously degrade device operation at critical dimensions as leakage happens. Hence, gate drain pull-in is undesired and rugged ohmic contacts are greatly preferred.

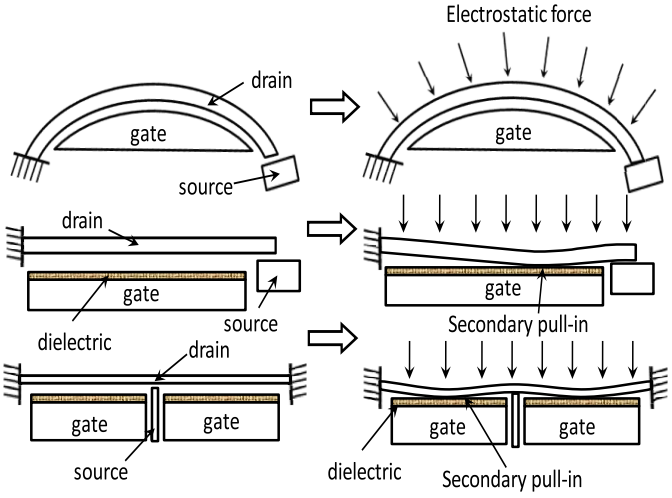

Fig. 1. Illustration of secondary pull-in comparison between electrostatic switch for curved beam, free-end cantilever beam and double-clamped beam.

The reliability of MEMS in vacuum have been investigated by several groups [21], [22]. The need for control of the environment around the switch is reinforced by reports

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of increased switch reliability while testing under vacuum [23]–[25], generally associated with a reduction in degradation due to oxidation and micro-welding [26], [27]. In this paper we propose a three-terminal, vacuum-encapsulated, curved beam switch defined in single crystal silicon, which is almost stress-free and homogenous. The entire moving structure and all electrodes are encapsulated in a vacuum environment with electrical interconnects built through the encapsulation to the chip surface and metalized by aluminum. These terminals consist of drain (movable curved beam), gate (fixed) and source (fixed) as shown in the top of Fig. 1. An arbitrary signal can flow through the contact from source to drain when the beam is pulled in electrostatically by the gate [28]. In order to increase the device's reliability through prevention of oxidation at the contacts, the switch is encapsulated in a process that eliminates residual O_2, hydrocarbons and water, leaving behind H_2 (the carrier gas during the seal) in the cavity at a sub-Pa pressure. Further, an ultra-clean environment is created as part of the *epi-seal* process [29], [30], as the wafer is exposed to high temperature >900 °C with hydrogen, dichlorosilane and hydrogen chloride. To reduce the contact resistance, a highly conductive layer can be coated on the contact of the switches. However, the high temperature conditions during the *epi-seal* process impose constraints on the materials allowed into the chamber to prevent contamination. In addition to the benefits of ultra-clean vacuum encapsulation, the curved beam design provides a high tolerance to a gate voltage overdrive. When the drain is in contact with source, the source acts as a stopper for the curved beam, and the curved shape of the beam reduces further deformation due to the arch-like structure, resulting in a robust configuration that is able to sustain a high gate voltage. This also increases the resilience to large overshoots during gate voltage pulses. These switches are highly suitable in rugged electronics applications such as downhole, aerospace and automotive applications. Regardless of the high contact resistance, logic devices and on-off circuits in harsh environments can be achieved.

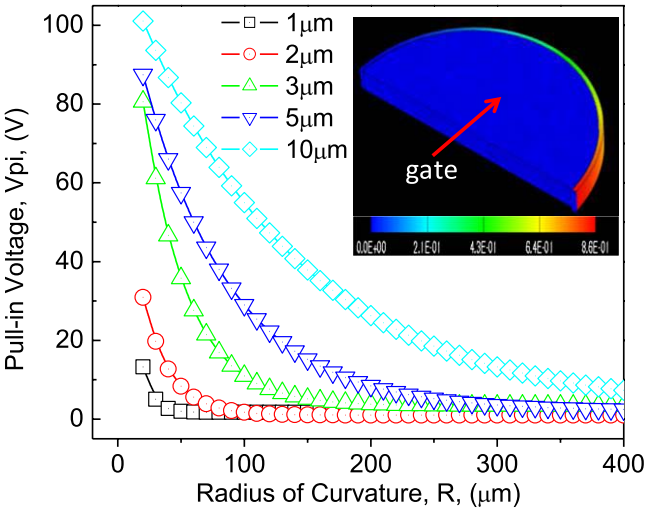

Fig. 2. Simulation result of pull-in voltage versus radius of curvature for curved beam with varying widths. Inset: 3D model of curved switch (Displacement: 0–0.86 μm).

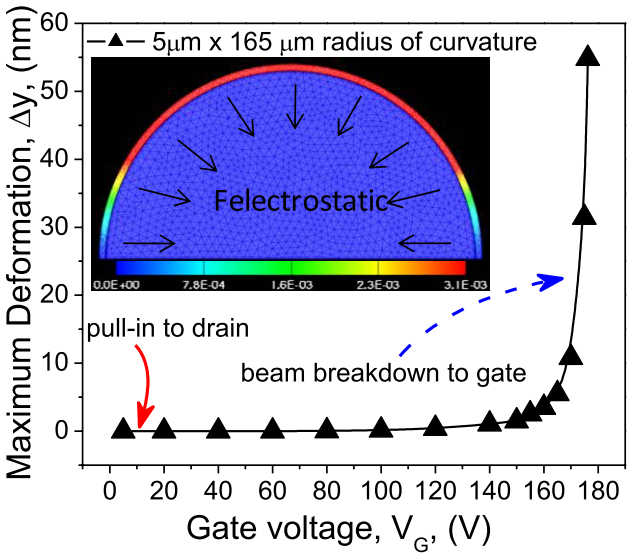

Fig. 3. Simulated high breakdown voltage of 174V with initial pull-in and contacted drain at approximately 11V. Inset: Pull-in of drain to gate during breakdown. (Displacement: 0–3.1 $\times$ 10^{-3} μm).

II. Design and Simulation

A. Finite Element Method Simulation

A 3D FEM simulation (Coventorware) model is used to simulate pull-in voltage for different beam length, widths, and radii of curvature. In this report, the modeled curved beam is a perfect semi-circle (shown in Inset of Fig. 2), and the length of the curved cantilever is given by the radius multiplied by π i.e. $l = \pi r$. Pull-in voltage (V_{PI}) can be obtained using Coventorware's CoSolve to solve both the mechanical and electrostatic physics domains. The electrostatic force is computed by applying a potential difference between gate and curved beam (drain). This force is then substituted into the mechanical domain to calculate the deflection. Iterating between these two domains yields a static solution at low voltage differences. When higher voltage differences are applied, the method no longer converges and iterations are performed to determine the minimum voltage at which no convergence is obtained, giving V_{PI}. Design rules for the *epi-seal* fabrication place a limit on device dimensions. The gap between drain and gate ranges from 1.0–1.5 μm and gap between drain and source is 0.7–0.8 μm. Gap distance is important in lowering pull-in voltage, which is proportional to gap$^{3/2}$. However, this gap has to be considered carefully as it is defined by etching unless some surface compensating process can be performed to fill the etching trench in order to make smaller gap [31]. As shown in Fig. 2, the simulated pull-in voltage is a strong function of the radius of curvature and the width of the beam, allowing us to tune the performance over a wide range with modest changes in these parameters.

In the breakdown voltage (secondary pull-in of drain-to-gate) simulation, a voltage ramp trajectory is applied to the gate and the beam's mechanical response is computed with a double clamped arch-structure as shown in the inset in Fig. 3. It is assumed that when curved beam contacts source, it becomes a double-clamped arch instead of a free-end

curved cantilever. As the beam deforms until a critical voltage, the growth of electrostatic force becomes dominant over the linear mechanical restoring force. This response is non-linear and numerous CoSolve iterations are performed to find a stable solution. A set of iterations are repeated between convergence and divergence of the solutions to determine the stable breakdown voltage of the arch structure. The breakdown voltage is thus determined in a similar manner as the pull-in voltage described above, with the exception of the double-clamped boundary conditions. The spring constant of the curved beam is expected to be approximately 16 times of a straight cantilever beam, resulting in very high breakdown voltage endurance. Simulation results of a 5 μm $\times$ 165 μm radius beam which has pull-in voltage of 11 V capable of withstanding excessive overdrive gate voltage and only breakdown at 174 V as shown in Fig. 3.

The vertical displacement, Δy, increases abruptly when nearing electrostatic pull-in. In these simulations, breakdown of the device happens when the beam is pulled in to gate near the center of the arch at relatively high voltage.

B. Modeling and Contact Dimple

Since the curved beam's width reported in this paper is much smaller than the radius of curvature, R $\gg$ h, the spring constant of the curved beam can be approximated by the curved beam deformation model [32], where neutral axis of the curved beam is parallel but not equal to the centroid axis. Assuming a uniformly distributed force, the spring constant of a curved beam, K_C is given by

$$K_C = \frac{2EI}{3\pi R^3(1-\alpha+\frac{\beta}{3})}; \quad \alpha = \frac{I}{AR^2}, \quad \beta = \frac{6EI}{5GAR^2} \quad (1)$$

where E is the Si Young's Modulus [33], I is the second area moment of inertia, R is the radius of curvature from centroid, A is the cross-sectional area of the beam and G is the shear modulus of elasticity. Subsequently, the pull-in voltage can be approximated by the parallel plate capacitor model, assuming negligible fringing effects, since the width-to-gap ratio is approximately (26:1) with largest gap being 1.5 μm, and the thickness of the device layer is 40 μm [34], [35].

The contact dimple is designed to reduce stiction while maintaining low operating voltage. As the spring stiffness is non-linear to its length and actuation gap, it is challenging to minimize the contact area to prevent stiction [36]. Surface forces and micro-welding between contact's asperities may be the cause of stiction. In this report, all of the curved switches have only a single and identical dimple.

Note that actuation of the curved switch is centripetal to the center of radius (0,0) and the radial electrostatic force is always tangential to the beam curvature. Therefore, rotating motion is considered when the curved beam is being actuated, with one side being anchored. The details of the contact design are shown in Fig. 4. The beam is attracted towards the gate by radial electrostatic force. After pull-in, the curved beam will assume a new position with a gap of g_o'. Hence, g_o has to be greater than the contact distance g_c to prevent short circuit between gate and drain. Thus, a multiplication factor x of 1.5

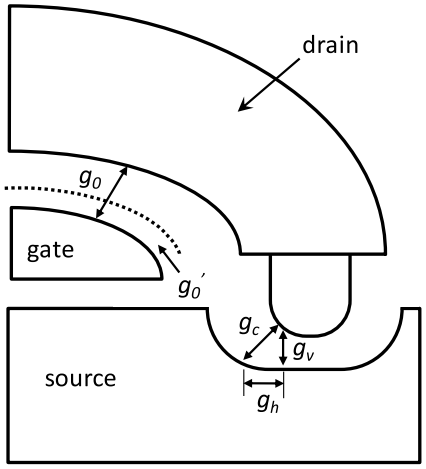

Fig. 4. Beam contact distance requirement for curved beam contacts.

is used throughout the design. The initial designed gap, g_o, is given by

$$g_o \geq x\sqrt{g_h^2 + g_v^2} \quad (2)$$

where g_o is the initial gap, x is multiplication factor, g_h is the horizontal distance between contact points and g_v is the vertical distance between contact points.

III. Fabrication and Process Flow

The *epi-seal* encapsulation process was proposed by researchers at the Robert Bosch Research and Technology Center in Palo Alto and then demonstrated in a close collaboration with Stanford University. This collaboration is continuing to develop improvements and extensions to this process for many applications, while the baseline process has been brought into commercial production by SiTime Inc.

The *epi-seal* fabrication flow is shown in Fig. 5 and described in detail elsewhere [37]. A silicon-on-insulator (SOI) wafer with a 40 μm-thick device layer and a 2 μm buried SiO_2 is used. First, deep reactive ion etching (DRIE) is used to form trenches through the device layer, stopping on buried SiO_2 layer. After that, sacrificial SiO_2 is deposited by low pressure chemical vapor (LPCVD) to overfill the trenches. In this regard the gap of the initial DRIE has to be limited that the etched trenches can be bridged over with oxide. Next, the deposited SiO_2 layer is etched to allow electrical contacts to the device layer. A first cap layer of epitaxial polysilicon is deposited and release holes are patterned and etched in it. Then, vapor hydrogen fluoride is used to release the oxide around the device. Subsequently the release holes are sealed by second layer of epitaxial polysilicon. During the sealing, the wafer is exposed to high temperature with a hydrogen gas carrier and this process removes most impurities, native oxide and polymers [38]. This results in a oxide-free Si to Si contact. Subsequently, electrical vias are defined in the cap, SiO_2 deposited, and finally the contact pads are opened and metalized with aluminum. The finished chip has flat topography and only the metal pads are visible under optical microscope. Nonetheless, scanning electron micrograph of a three terminal curved beam switch before capping is shown in Fig. 6.

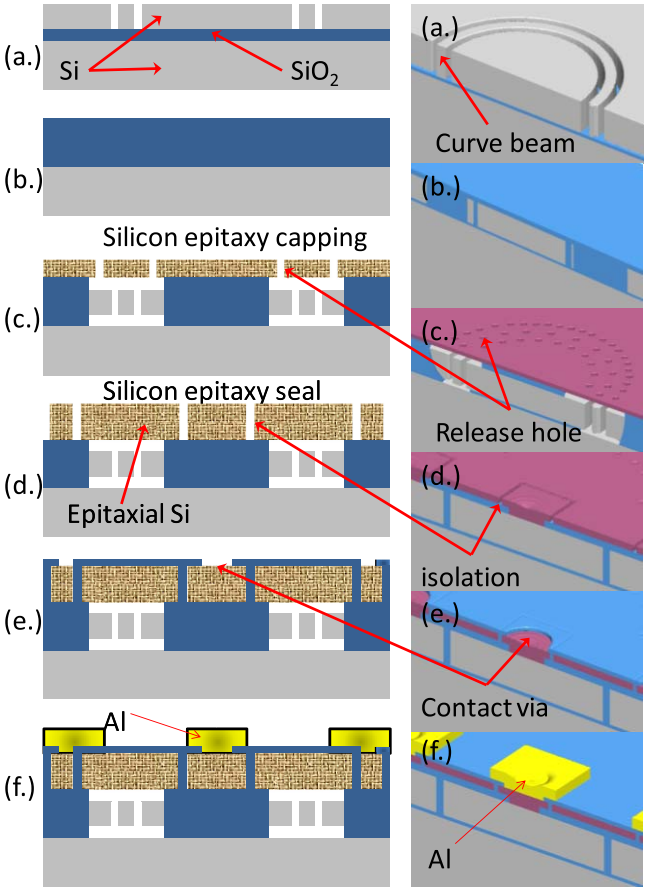

Fig. 5. Fabrication process flow. (a) Si deep trench etching. (b) Deposited SiO_2 bridges over the trenches. (c) Vent hole definition with device release. (d) Epitaxial polysilicon sealing and electrode isolation. (e) Passivation opening. (f) Al metallization.

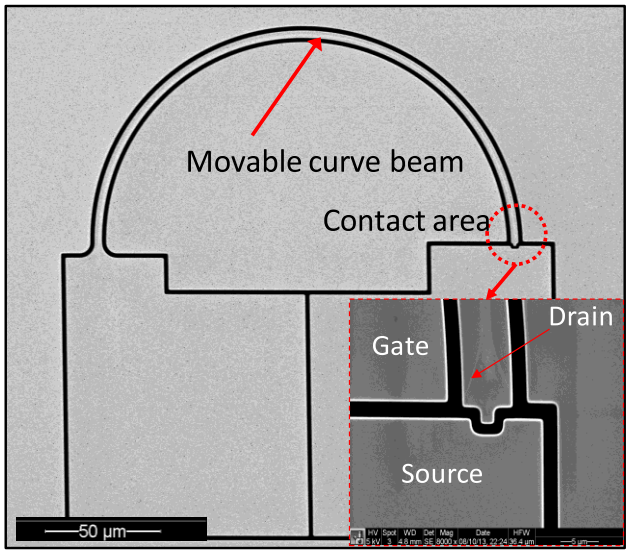

Fig. 6. Scanning electron micrograph (SEM) of a 3 μm × 85 μm radius curved switch. (Inset) Zoom-in of the contact region.

The cross section of encapsulated curved beam is shown in Fig. 7. A protruding silicon curved beam is shown in Fig. 7(a). Note that during the *epi-seal* process, the DRIE etched surfaces are smoothed under a silicon reflow process

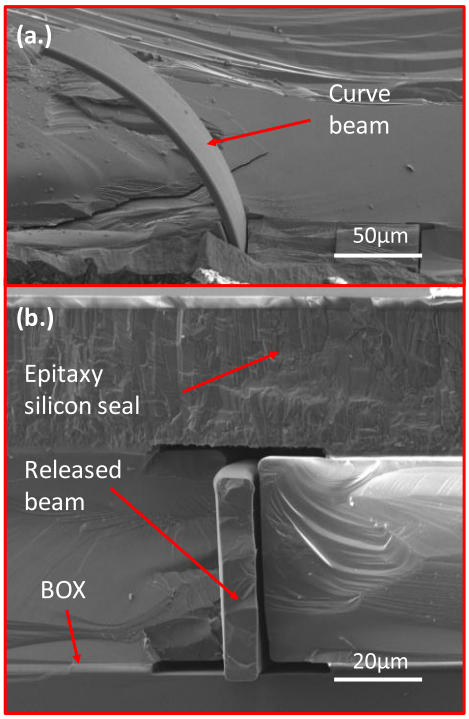

Fig. 7. SEM cross section of a curved switch device showing the released curved beam with a polysilicon encapsulation seal. (a) Encapsulated curved beam. (b) Epi-seal process with encapsulated beam.

as reported [39]. The released beam is encapsulated under a ~25 μm-thick epitaxial polysilicon layer, as shown in Fig. 7(b).

IV. Testing Set-Up

The fabricated switch is tested under two different conditions: 1) room temperature (~25 °C) in air at atmospheric pressure, and 2) an elevated temperature of 300 °C in nitrogen. At room temperature, the chips is exposed to air and tested in a Cascade Microtech microchamber (RBL-6100) with Agilent semiconductor analyzer B1500 equipped with two standard source monitoring units (SMU) and one high resolution (HRES-SMU). Meanwhile, testing at the elevated temperature of 300 °C is carried out in another test chamber with temperature controller in a Cascade Microtech vacuum probe station (PMV200) using the same electrical setup. The enclosed environment of the vacuum probe stations enable the chamber to be purged and filled with nitrogen. This is meant to protect the interior and hardware of the probe station when the temperature is raised to 300 °C. The switch, however, operates within the *epi-seal* encapsulation in a hydrogen environment, and is subject largely to the temperature effects of the two test conditions. Finally, switching delay of the device under 300 °C is measured using Keithley SCS-4200 equipped with one 4225-PMU high speed pulse IV module.

V. Experiment Results and Discussion

A. Gate Voltage Sweeping

Fig. 8 shows the typical measured pull-in and pull-out curve of a 3 μm wide × 75 μm radius curved beam switch.

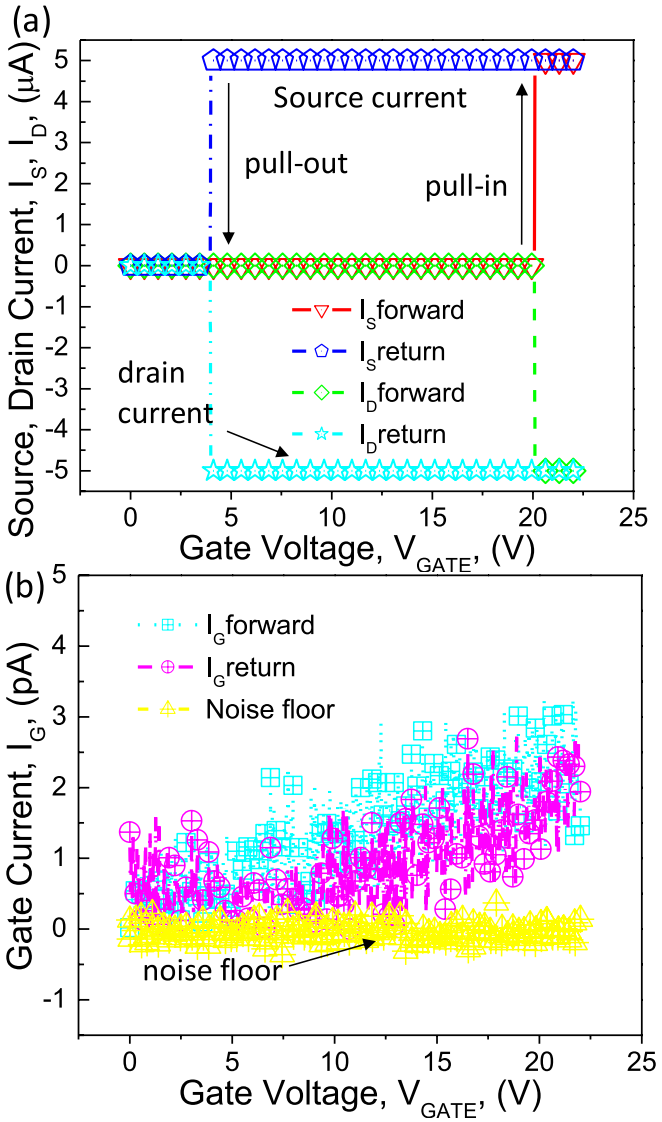

Fig. 8. Three terminal testing of I_D, I_S, I_G–V_G. (a) Switch turns on during forward V_G sweep and turns off during return V_G sweep. (b) I_G remains low with measured noise floor of the analyzer.

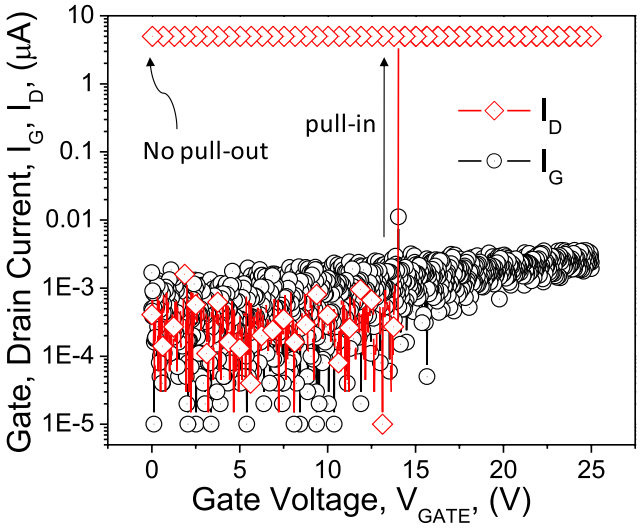

Fig. 9. I_D, I_G–V_G of 5 μm wide × 165 μm radius curved beam. Permanent non-resettable contact is obtained.

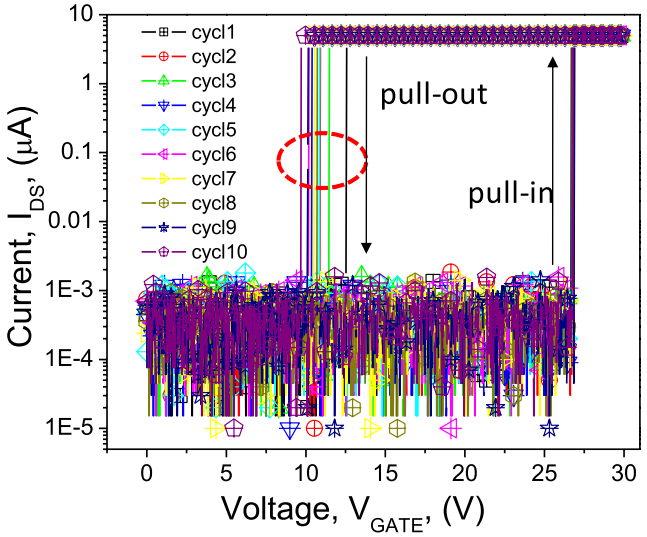

Fig. 10. Measurement of ten sweeping cycles. I_{DS}–V_G sweeping cycles within same device. Pull-out variation is highlighted.

The gate voltage (V_G) is swept from 0 V to 25 V. The pull-in phenomenon is indicated by an abrupt drain (I_D) and source current (I_S) rise as indicated during the voltage increment sweep, while pull-out voltage is represented by the abrupt drop in both current during voltage decrement sweep. This is shown in Fig. 8(a). In this switch, the pull-in voltage (V_{PI}) is 20 V and pull-out voltage (V_{PO}) is 4.77 V. A three-terminal device is demonstrated with low gate current (I_G) throughout the measurement as shown in Fig. 8(b). In this measurement, all three currents: drain, source and gate currents are measured. A voltage sweep is applied to the gate, with a DC bias of 2.5 V applied to the source and subjecting the drain to ground. As the drain contacts the source, a current flow from the source to the drain, and this current is limited to 5 μA to protect the contact from excessive joule heating. Measured current on-off ratios (*Ion/Ioff*) from 10^4 to 10^7 and subthreshold swing of approximately 6.25 mV/decade are demonstrated. V_{PO} can be measured by sweeping the gate voltage from 25 V to 0 V. The hysteresis window in pull-in and pull-out voltage is related to the surface adhesion and the nonlinearity in electrostatic force caused by the pull-in. In order to break-off from the contact, the spring restoration force has to overcome surface adhesion and electrostatic force. The gap between the pull-in and pull-out can be seen as a measure of the balance between spring constant and surface adhesion force. It is noted in these experiments that most low voltage designs (<15 V) only work once and no pull-out can be detected. Such a result is shown for a 5 μm wide × 165 μm radius curved beam (Fig. 9). After one pull-in, we found that the curved beam is permanently in contact. Although surface adhesion such as van der Waals force and surface charging, the permanent contact may have been caused by micro-welding due to joule heating at the asperity-to-asperity contact, as this effect is consistent with the increasing of the current limit in the source-drain terminal.

For most devices that actuate at higher voltages, the curved switches produce a consistent V_{PI} within same device. Ten cycles of repeated gate voltage sweeps are shown in Fig. 10, indicating a consistent pull-in voltage at

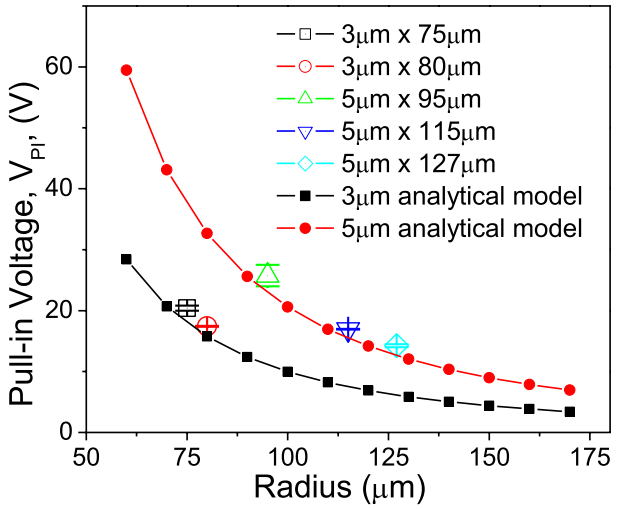

Fig. 11. Comparison between measured pull-in voltages (V_{PI}) of 3, 5 μm (width) curved beam with various radius versus analytical model.

approximately 26V for a 5 μm wide $\times$ 95 μm radius curved beam, while the average pull-out voltage is 11.9 V. The gate current (I_G) remains low throughout the measurement in fA range. The observed variation in the pull-out voltage is related to the adhesion force between contact surface of drain and source, which can evolve somewhat due to wear of asperities [41].

Overall, the pull-in voltage (V_{PI}) is agreeable to the analytical model as shown in Fig. 11, a total of experiment results of 15 devices were tested and compared to the analytical solution. Absolute error of 1V–3 V is confirmed with the devices tested.

B. Gate Voltage Stress Test

Fig. 12 shows the stress testing of the curved beam by overdriving gate voltage (V_G) well beyond the pull-in voltage (V_{PI}) of two respective devices. While abrupt switching characteristics of drain-source current (I_{DS}) equivalent to current on-off ratio (*Ion/Ioff*) of 10^7 is observed, the gate current (I_G) remains low in fA range throughout the voltage sweep from 10 V to 50 V for a 5 μm $\times$ 95 μm radius curved beam. The pull-in voltage of this device is 24.5 V as shown in the measurement in Fig. 12(a). A similar result is obtained from another device with 5 μm $\times$ 115 μm radius beam with a lower pull-in voltage of 15.5 V. No breakdown is observed at gate voltage (V_G) sweeps from 0 V–100 V, which is the maximum voltage setting of the test equipment. High breakdown voltages have also been reported with an inclined curved electrode with rotation around small hinges [41]. However, such hinge placement imposes higher flexibility in horizontal x-direction and may cause breakdown earlier than a perfect circular beam. High overdrive voltages can impose large contact forces on the switch and may result in more severe mechanical degradation at the contact surface, hence causing early fatality. There is also a probability that the switch could become stuck with no pull-out detected after a very high gate voltage overdrive.

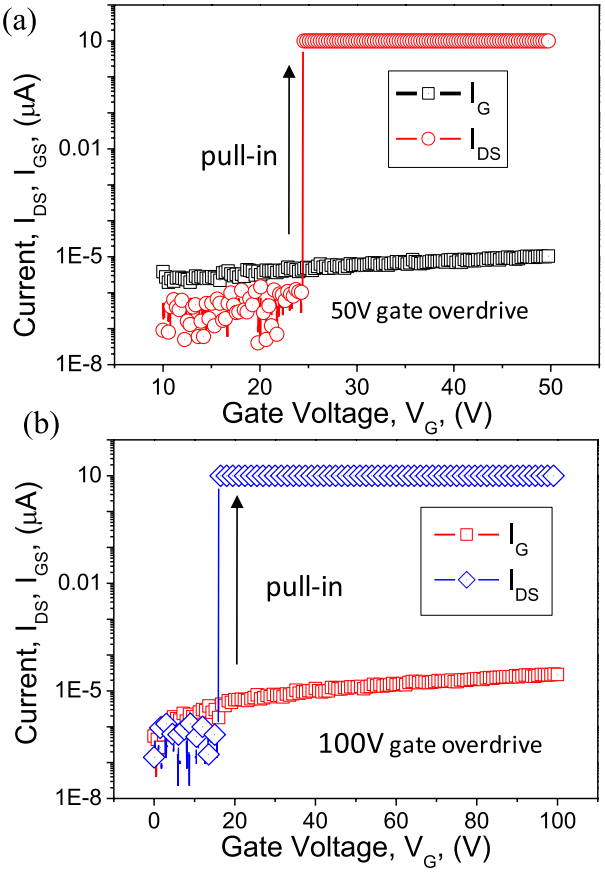

Fig. 12. High voltage breakdown endurance. (a) V_{PI} at 24.5 V of 5 μm $\times$ 95 μm radius beam, V_G until 50 V. (b) V_{PI} at 15.5 V of 5 μm $\times$ 115 μm radius beam, V_G until 100 V.

TABLE I
PARAMETER SETTINGS FOR ON-OFF CYCLE

State	Parameters		
	Gate bias (V_G)	Source bias (V_S)	Current limit (I_{DS})
On-cycle	$\geq V_{PI}$+ 1V	2.5V	compliance = 5nA
Off-cycle	0	2.5V	compliance = 5nA

C. Room Temperature Cycling

A real time measurement was performed using two different test states in the semiconductor analyzer. The first state turns on the device by setting gate voltage above the pull-in voltage by 1 V to ensure that the switch turns on. The second state resets the device by setting the gate voltage to zero bias, turning the switch off. Finally both states can be looped to a desired number of cycles. One cycle consists both on and off test states. Three parameters, the currents (I_{DS}, I_G) and the bias voltage (V_G) were recorded. The source bias (V_S) is set to a low voltage of 2.5 V, to provide current signal flow from source to drain. The current compliance of I_{DS} is set to 5 nA, in order to protect the contact from excessive joule heating due to high current. The on-off cycling conditions are illustrated in Table I.

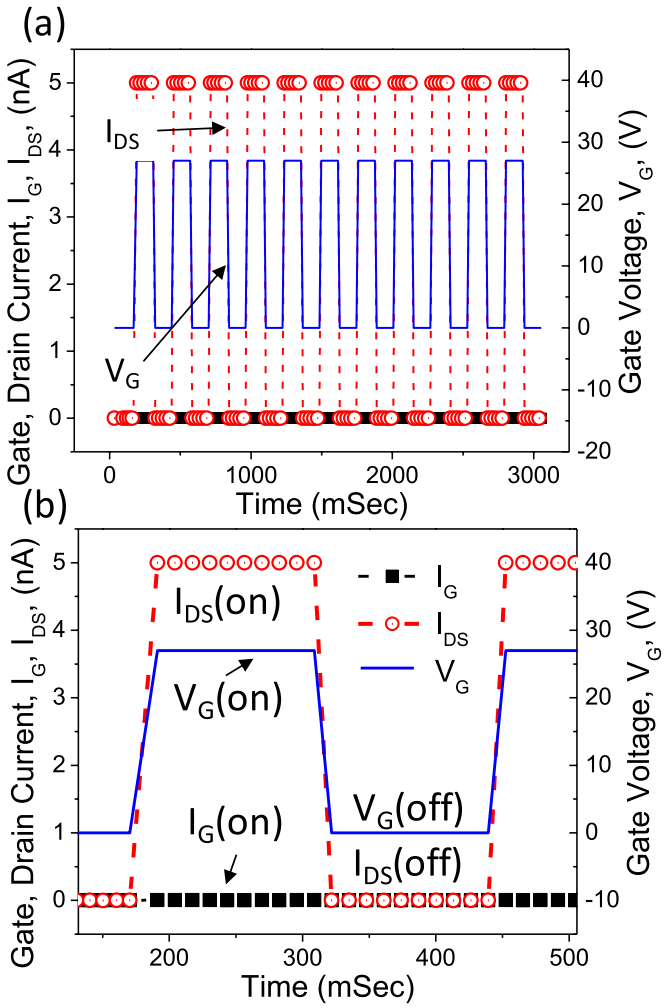

Fig. 13. Real time measurement set-up for on-off cycling test up to 10^5 cycles under ambient condition of 5 μm $\times$ 95 μm radius beam. (a) Real time measurement of multiple cycles. (b) Zoom-in of one cycle.

Despite the simple settings, the operational characteristics of the semiconductor analyzer induce delays of a few seconds between loops. Hence measurement of 10^5 cycles consumes approximately 100 hours to complete. Every on-off cycle records 10 samples within sampling interval period of 400 mSec, which translates to 2.5 Hz, which is still far away from the simulated resonant frequency of 111 kHz. Assuming ~25 μSec switching delay, the contact and hold time for each cycle is approximately 200mSec. This results in a total contact time of approximately 5.5 hours under ambient temperature condition for 10^5 cycles for these tests. Note that all switching cycles were performed under hot switching contact mode, where source signal is biased at 2.5 V (5 nA compliance) during the on-off cycles. Fig. 13(a) shows the real time measurement of multiple cycles of a 5 μm $\times$ 95 μm radius beam. During the on-state, a source-drain current (I_{DS}) flows when the curved switch is turned on by gate voltage (V_G), which is set 1 V higher than the pull-in voltage (V_{PI}). More details are shown in Fig. 13(b). During off-state, I_{DS} drops to near zero almost immediately when gate voltage is turned off. It is also important to verify that both on and off gate current remain low in fA range. Overall,

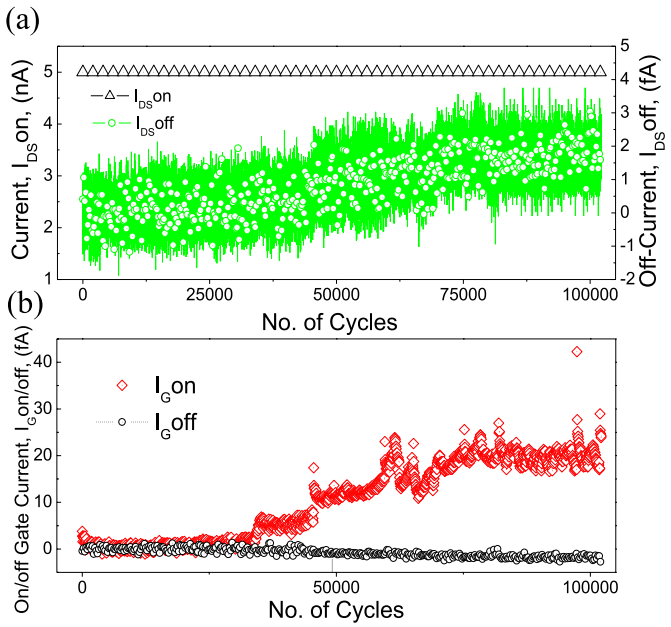

Fig. 14. I-V characteristics for 10^5 cycles under ambient condition. (a) On-Off drain source current, I_{DS} versus number of cycle. (b) On-Off gate current, I_G versus number of cycle.

the behavior is similar to an ideal three-terminal logic switch switching device [42].

The lifetime of MEMS switches depends on the operating environment. Lower performance, reliability and failure can be caused by factors such as humidity, heat, pressure and stiction. In this work, we have demonstrated some preliminary reliability results of a MEMS switch operating in high temperature environment. 10^5 room temperature cycles is performed with each cycle observed. Since each cycle of on and off is being recorded, the I-V characteristics of both drain-source current (I_{DS}) and gate current (I_G) during each on and off cycle can be obtained. Data extracted from the measured I-V characteristics of every cycle are shown in Fig. 14. In each cycle, the drain-source current, (I_{DS}) reaches the 5 nA current compliance limit in the on-state. In the off-state, the leakage current between the drain-source and the gate-source contacts is in the fA range. During experiments up to 10^5 cycles, there is some gradual increase in the leakage current between the open drain-source and gate-source contact. This source has not been identified, but could include leakage between the electrodes on the surface of the chip, internal leakage due to wear at the contacts. Experiments are being considered to identify this leakage source.

D. Cycling at 300 °C

A 5 μm $\times$ 95 μm radius device is verified to work at least for 10^4 cycles at an elevated temperature of 300 °C. The measured result is comparable to the initial cycling condition of cycling results at room temperature. A 5 μA current with a large voltage bias is set across source and drain. As the switch turns on, this current flow through the source-drain terminal and the voltage will adjust itself to maintain maximum current of 5 μA. This voltage bias is measured by the source monitoring unit and the contact

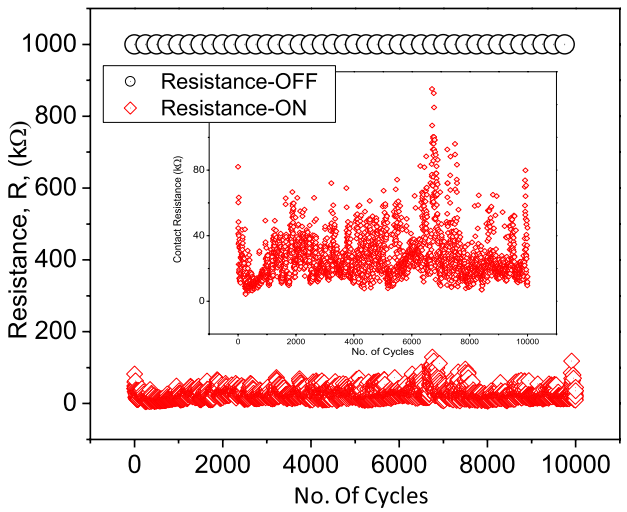

Fig. 15. Contact resistance versus no. of cycles under 300 °C elevated temperature. (Inset) Zoom in on the contact resistance during on cycle.

resistance can be directly extracted. The current compliance setting is important in this experiment as too high current may cause excessive joule heating and the switch may fail. Fig. 15 shows the measured contact resistance during the cycling of this device. The contact resistance remains average ∼28 kΩ throughout these tests. The large deviation in the contact resistance is a result of the contact asperity modification after every on-off cycle. Note that when device is turned off, the measured contact resistance of 1 MΩ represents saturation in the measurement. The actual open circuit resistance is known to be in hundreds of gigaohms. The main result of this experiment is confirmation that the switch remains stable up to 10,000 cycles, even when operated at 300 °C.

E. Curved Beam Switching Speed

The switching speed of the curved beam switch is extracted through ultra fast I-V pulse monitoring unit using Keithley SCS-4200 semiconductor analyzer. A fast pulse of 27 V, 100 nSec rise/fall time with a 50 μSec pulse width is applied on the gate bias voltage (V_G) to turn on switch while another pulse with lower voltage, 2.5 V, same rise/fall time with larger pulse width of 60 μSec is applied to the source (V_S). V_S has larger pulse width so that the source voltage encompasses the entire gate voltage pulse, which enables the measurement of entire switch on and switch off in the curved beam. Both the source-drain current (I_{DS}) and gate current (I_G) are monitored during the pulses. Fig. 16(a) and (b) shows the real time on-off switching delay of 5 μm × 75 μm radius and 5 μm × 95 μm radius curved switch respectively. Under vacuum encapsulation, squeeze film damping is considered insignificant in switching delay. The on-off delay of the beam is due to charging, inertia, switch bounce, and finally, surface adhesion. The calculated spring constant K_C of the 5 μm × 75 μm radius and the 5 μm × 95 μm radius curved beams are 58.7 N/m and 39.8 N/m respectively. Between these two examples, a faster switching speed is detected in a shorter curved beam due to higher spring constant, which is consistent with a standard resonant model [43]. Note that there is a few μSec delay switch off in the 5 μm × 95 μm beam. This is probably the delay when the beam breaks the contact, which is held by surface adhesion, surface charges and micro-welding.

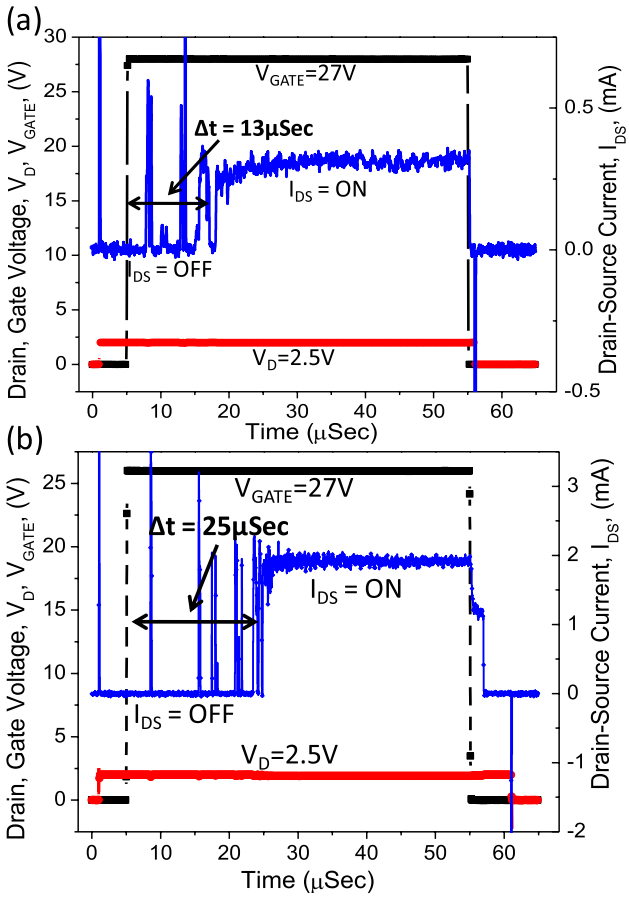

Fig. 16. Ultra high speed pulse I-V measurement for switching delay. (a) 5 μm × 75 μm radius switch. (b) 5 μm × 95 μm radius switch.

VI. Conclusion

In summary, an encapsulated curved beam silicon switching device is designed, fabricated and characterized. Both simulation and experiment show that the curved beam has potential for mitigation of secondary pull-in, thus enabling a robust threshold voltage in switch operation. Besides that, reliability of such vacuum encapsulated switch is demonstrated and the switch is proven to work at least for 10^5 cycles under ambient condition and at least 10^4 cycles under elevated temperature of 300 °C. Micro-second switching delays are measured, showing fast switching of 13 μSec from off to on, and immediate switch off. This switch has potential for complementary CMOS-MEMS devices, power gating applications and high temperature rugged electronics.

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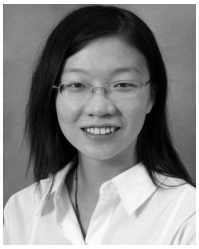

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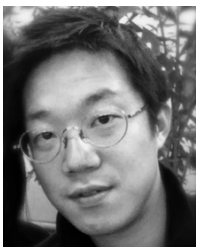

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