Tantalum-Nitride Antifuse Electromechanical OTP for Embedded Memory Applications

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***Abstract*— Embedded nonvolatile memory (NVM) integrated in the back-end of line processes are of high interest, particularly for rugged environments (high temperature/radiation or vibration). This letter demonstrates the use of tantalum nitride microbeams as antifuse one-time programmable (OTP) NVM. It needs a single mask process and can be integrated above an integrated circuit. Typical fusing current is 1 mA, operating voltage is 4 V, and the measured contact resistance is <2 kΩ. A hybrid one-transistor/one microbeam/bit memory array is proposed for back-end compatible and low-cost OTP NVM integration.**

***Index Terms*— Embedded memory, nanoelectro-mechanical systems (NEMS), nonvolatile memory (NVM), one-time programmable (OTP), tantalum nitride (TaN).**

I. Introduction

EMBEDDED nonvolatile memory (NVM) integrated on top of CMOS wafer is an essential part of modern integrated circuits. The leading NVM technology is based on floating gate transistors, which, however, have limited performances when exposed to high temperature ($T > 200$ °C) [1], mostly because of charge leakage. Various designs of storage-layer-free electromechanical NVM actuated by electrostatic forces are proposed [2]–[4]. Data retention is typically obtained by adhesion forces between two smooth surfaces in contact [5].

Bistable electromechanical nonvolatile structures are, however, difficult to be integrated in a compact fashion and with low-voltage actuation. Therefore, one-time programmables (OTPs) [4]–[6] are proposed, especially for rugged applications (high temperature, rad-hard, and high vibrations). The antifuse geometry proposed in this letter consists of a two-terminal structure: one movable beam and one fixed electrode. Upon application of a dc voltage to the movable beam, it will deflect and eventually get fused to the fixed electrode (Fig. 1). Memory reading is achieved by probing the conductance between the two electrodes, having an ideally large ratio between the original opened state (bit 0) and the fused state (bit 1). This letter proposes the fabrication process, electrical measurement, and memory array design of OTP NVM based on tantalum nitride (TaN) microbeams.

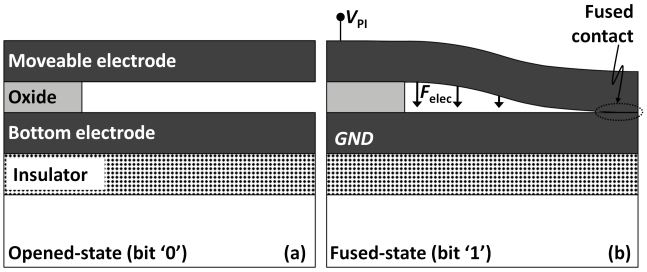

Fig. 1. Cross-section principle of the proposed OTP NVM in the (a) opened- and (b) closed-states. Long beams are ideal for closing the gap with a large contact area.

II. Process Integration

The one-mask process is integrated on bulk 8″ silicon wafer. The following layers are successively deposited: 200-nm low-pressure chemical vapor deposition nitride (SiN) as insulator, 200-nm TaN as fixed electrode, 150-nm plasma-enhanced chemical vapor deposition (PECVD) silicon dioxide (SiO_2) as sacrificial layer, and 200-nm TaN as movable electrode. The stack needs to be annealed at $T = 900$ °C during $t = 5$ min under N_2, to manage the stress of the metal. A double hard mask consisting of 300-nm PECVD silicon dioxide and 600 nm of PECVD amorphous silicon (a-Si) is then deposited.

After photolithography, amorphous silicon is etched and the photoresist is stripped. Then, a-Si patterns are transferred to the oxide hard mask, and finally to the top TaN electrode. The double hard-mask process guarantees that the metal will never be exposed to photoresist, and therefore the whole process will be free of organo-metalic residues. TaN is dry etched with HBr/Cl $_2$ gas, at a power of 1300 W and a partial pressure of 1.7 mTorr.

Initially, the release comprises removing the amorphous silicon in a tetramethylammonium hydroxide (TMAH) tank (Fig. 2), then dipping the wafer in a diluted HF bath (1:100) to clean the surface of oxide from dry etching residues, and finally, releasing single-clamped beams in a vapor-HF chamber to prevent permanent stiction between the movable and the fixed electrode. As the etching time for the particular vapor-HF recipe strongly affects the undercut distance, it must be controlled to avoid over-release of fixed electrodes (Fig. 3). Four-point measurement of annealed TaN is conducted and

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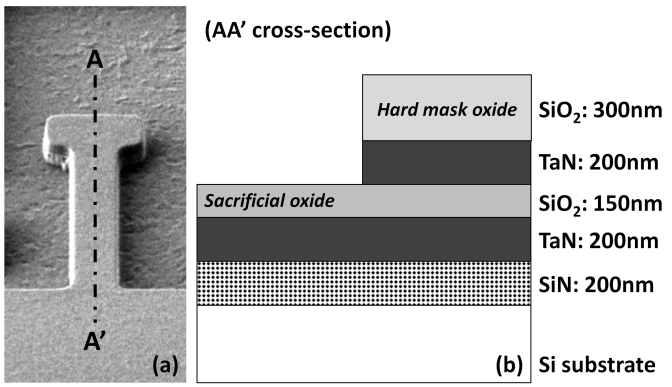

Fig. 2. (a) SEM of the storage device during the fabrication process and (b) corresponding stack of material used.

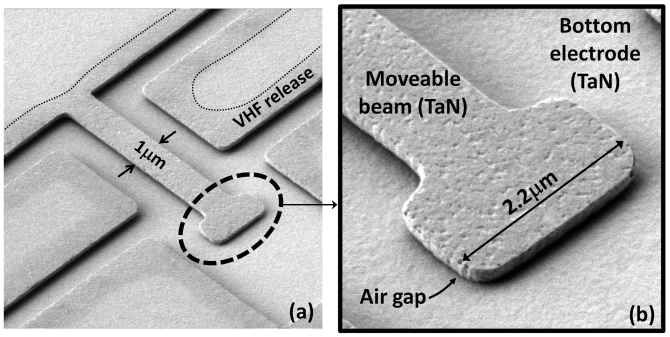

Fig. 3. (a) SEM of a hammer-head TaN memory beam. (b) High-magnification zoom in the head portion of the beam where fusing happens during writing. Residual prestress is visible.

a value of $4.6 \cdot 10^{-5}\ \Omega$·m is extracted, in good accordance with other reports [7]. TaN is widely used as antidiffusion barrier in Cu interconnect technology back-end-of-line (BEOL), and is therefore an ideal metal for BEOL NVM [8]. In addition, TaN beams do not oxidize quickly when exposed to air, making them useable even if not packaged under vacuum.

III. Memory Programming and Storage

Samples are annealed at $T = 120$ °C before testing, to make metal surface free of moisture. Then, electrical testing is conducted at room temperature under N_2 ambient. More than 50 devices are successfully measured. A sweep dc bias is applied to the beam, whereas the bottom electrode is grounded. At $V_{\text{beam}} = V_{\text{PI}}$ (pull-in voltage), the beam will collapse toward the fixed electrode and shorts the two electrodes. In particular, the current is limited by the compliance value of the parameter analyzer (Fig. 4).

Once fused, the beam will not go back to its idle position and remains permanently fused to the bottom electrode. Beam geometries of 5.4-μm long × 1-μm wide × 200-nm thick have a pull-in voltage ranging from 3 to 3.5 V, enabling low-voltage switching.

Using classic formulation of the pull-in voltage of a single-clamped beam [9], and $E = 350$ GPa as TaN Young's modulus, the single-clamped design of Fig. 4 is calculated to have an equivalent elastic constant of 4.5 N/m, corresponding

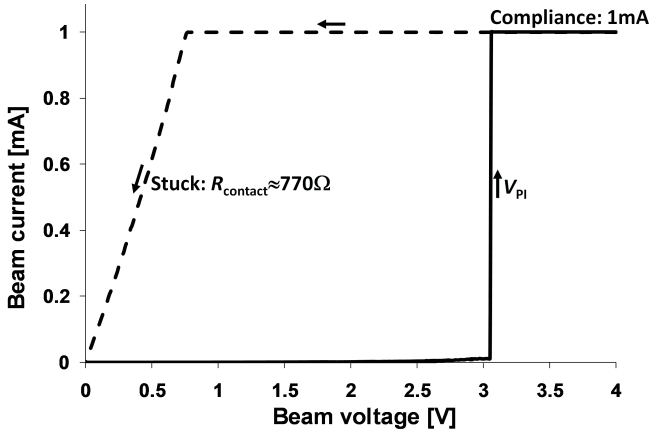

Fig. 4. Writing characteristics of a 5.4-μm long and 1-μm wide TaN OTP beam. Current dc compliance is 1 mA, and measured pull-in voltage (V_{PI}) is 3.05 V. Once fused, the measured switching resistance is 770 Ω.

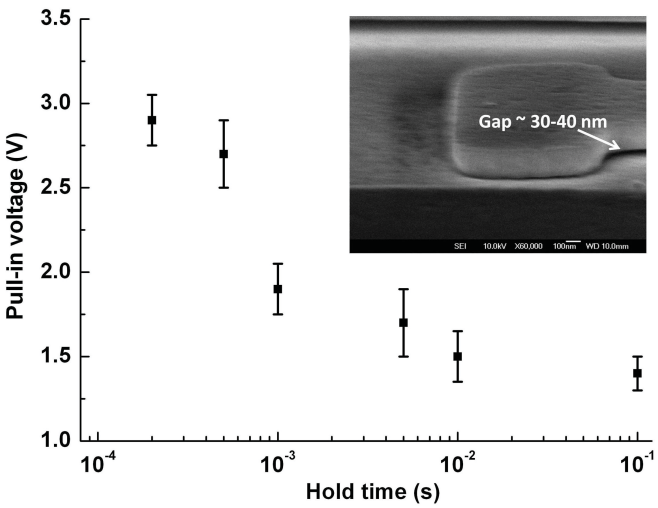

Fig. 5. Measured pull-in voltage for different individual switches fused with different hold time during dc sweep (200 μs–100 ms). The XSEM image (inset) confirms the actuation gap in the range of 30–40 nm.

to a theoretical pull-in voltage typically 3× higher (9.7 V) in comparison with measured data. The residual warpage caused by TaN stress and undercut (during the dry HF release) of the beam results in smaller actuation gap (see Fig. 5 inset) and thus reduce the actuation voltage.

Once fused, the I–V characteristic is linear and only limited by current compliance. The switch dimension and the conductivity of TaN suggest that the movable to bottom electrodes resistance can be approximated by the contact resistance R_{contact}. All fused beams are found to remain closed when further probed.

Multiple devices are programmed with a current compliance ranging from 0.1 to 2 mA. It is observed that a current < 0.1 mA may result in insufficient fusing, and the memory bit going back to its opened state. At the contrary, a high fusing current (I>2 mA) will blast the beam. For different current compliance (0.1–2 mA), no clear trend is observed for the on-resistance and it is observed to be in a range from 100 Ω to 2 kΩ. Results plotted in Fig. 5 show that the pull-in

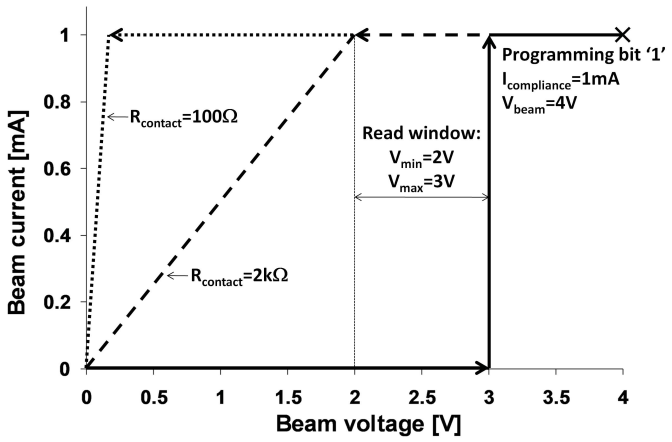

Fig. 6. Suggested operating mode of the OTP NVM proposed. Switching $0 \rightarrow 1$ is achieved by fusing the switch at $V = 4$ V and $I = 1$ mA (corresponding to $V_{\rm PI} + 1$ V). A 1-V reading window is available, with excellent distinction between bit 1 ($I = 1$ mA) and bit 0 ($I = 0$).

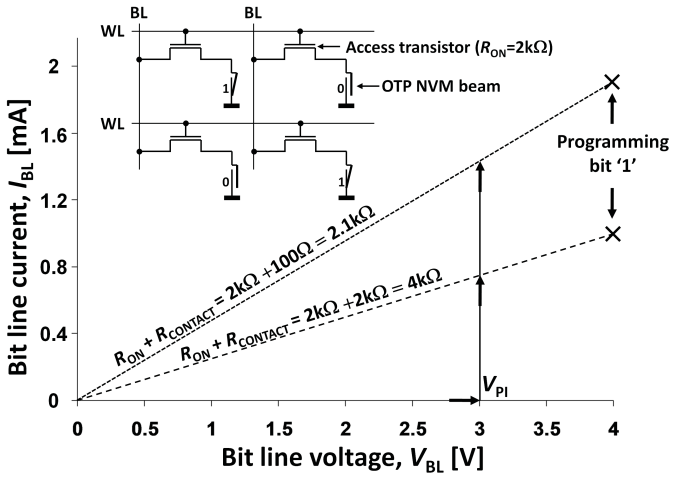

Fig. 7. Proposed one-transistor one-MEMS NVM array. An NMOS in saturation mode is used to both fuse and read the memory. A transistor with $I_{\rm DS\_SAT} = 2$ mA is ideal as a self-limiter current device.

voltage depends strongly on the hold time during the dc sweep. In particular, a higher pull-in voltage ($V_{PI} \sim 3$ V) is obtained when hold time is short ($T_{\rm HD} = 200\ \mu$s) compared with lower pull-in voltage ($V_{\rm PI} \sim 2$ V) at $T_{\rm HD} = 100$ ms. Although capacitances are relatively small for the charge induction, the higher pull-in voltage at smaller hold time may be attributed because of the capacitive shunting effect.

In addition, the square pulse is applied through bottom electrode to actuate the suspended beam and to compare the pull-in voltage with dc sweep. A square-shaped input signal (pulsewidth $= 10\ \mu$s) with amplitude of 3.0 V is adequate to fuse the beam and output signal at the drain electrode is monitored with the oscilloscope to record the switching speed. The time for switching on the device is found to be 1.26 μs. The switching speed is further reduced by choosing the higher amplitude of the square-shaped input signal (700 ns for 6 V). The switching speed is faster than a commercial flash memory and can be improved by further increasing the pulse amplitude or reducing the MEMS switch dimensions.

IV. Nonvolatile MEMS Memory Array

Measured data demonstrate the use of TaN beams as OTP NVM. Fig. 6 shows that despite the variation in the contact resistance, bits can be programmed at $I = 1$ mA, and read in the $V_{\rm min}$–$V_{\rm max}$ window. This programming tolerates variation in the pull-in voltage, typically ranging from 3 to 3.5 V.

Fig. 7 proposes a one-transistor/one-MEMS design for the implementation of NVM arrays. The same NMOS transistor is used as a current limiter for the one-time writing operation ($0 \rightarrow 1$) and as access transistor to read the memory. Typically, a transistor with $R_{\rm ON} = 2\ \rm k\Omega$ is ideal to limit the current and make sure the beam is fused within a proper current range. The design shows that a memory density of $\sim 150\ \rm kbit/mm^2$ is easily achievable.

V. Conclusion

This letter proposed a new design of antifuse OTP NVM based on single-clamped TaN microbeams. The process was back-end compatible and required only one photolithography mask. A typical 1-mA fusing current was needed to achieve permanent adhesion. The device operated at 4 V, which made it ideal for low-power applications, and it could be efficiently switched and read by an NMOS transistor. Further work should include testing under rugged conditions, and optimal stress management of TaN. Scaling down of the structure, as well as process optimization for reliable BEOL integration, is also needed.

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