A Junctionless Gate-All-Around Silicon Nanowire FET of High Linearity and Its Potential Applications

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***Abstract*—The linearity of a gate-all-around junctionless silicon nanowire (SiNW) FET has been analyzed. The SiNW FET shows a perfectly linear I_D–V_G relation and a nearly zero output conductance. The mechanism of its linear behaviors due to degenerate doping level has been also demonstrated. For RF applications, the proposed SiNW FET exhibits a much lower distortion for a whole range of load resistance, making it superior to modern short-channel MOSFET.**

***Index Terms*—Third-order intermodulation (IM3), linearity, silicon nanowire (SiNW) FET.**

I. Introduction

LINEARITY is a crucial figure-of-merit for both analog and radio-frequency (RF) circuits. A high linearity is desired as signals should be linearly amplified so as to exhibit no distortions. For RF circuits, linearity is much more crucial. Nonlinearity may induce intermodulation (IM), which will generate signals with frequencies different from the input ones. These unwanted signals may fall into the band of interest, interfering or even corrupting the desired components [1]. However, MOS transistors are inherently not quite linear. Conventional long-channel MOSFET obeys the square law, which deviates much from linear drain current versus gate voltage or I_D–V_G relation. Although modern small-feature size MOSFET exhibits a linear relation, improvements from it can be very limited due to the short-channel effects. To achieve high linearity, carefully designed sophisticated circuits are employed to minimize the nonlinearities from MOS transistors [1]. This methodology will definitely enlarge the IC area and power consumption and is therefore a high cost solution.

Another approach to achieve high linearity is to minimize the inherent nonlinearities of the transistor itself. Since transconductance and output conductance are two dominant nonlinear sources [2], a high-linearity transistor requires both small size and minimum short-channel effects. Recently, the gate-all-around junctionless silicon nanowire (GAA JL SiNW) FET has become a promising transistor device for its relatively simple process flow and high performance [3]. This kind of SiNW FET can simultaneously satisfy the two requirements for high linearity due to its nanoscale feature size and immunity to short-channel effects [3]. Unfortunately, as far as we know, there is no reported linearity analysis of the SiNW FET.

In this letter, the linearities of two n-type GAA JL SiNW FETs at different doping levels are investigated. The degenerately doped SiNW FET is found to exhibit an inherently low nonlinearity. A possible theory is employed to explain the underlying principle. The potential application in RF circuits is evaluated as well.

II. Development and Characterization

A 1170-Å-thick device layer on top of a 1450-Å oxide layer of a silicon-on-insulator substrate is first implanted using phosphorus with a dosage of 4×10^{15} cm^{-2}. Then, patterns with critical dimension of around 90 nm in width are formed and followed by a 5-h thermal oxidation in order to shrink down the internal SiNW diameter to around 10 nm. The length of SiNWs is about 400 nm. After removing the oxide surrounding the SiNW using buffered HF solution, a 40-Å thin oxide is formed as the insulator of the device. Then, 4000-Å polysilicon is deposited, heavily doped, and patterned to serve as the gate, as illustrated in Fig. 1(a) and (b). Furthermore, a 4000-Å Plasma-enhanced chemical vapor deposition (PECVD) oxide is then deposited as a passivation. The electrical traces are formed after via opening and metal deposition. Finally, 1-μm PECVD silicon nitride layer is deposited on top, and the pads are opened for testing. Another wafer with the device layer of intrinsic doping has been also fabricated as reference following the aforementioned process. The two SiNW FETs with a doping concentration of 10^{20} cm^{-3} and intrinsic doping are denoted as FETs A and B, respectively.

The transfer characteristics of FETs A and B at a drain voltage of 1.5 V are shown in Fig. 1(c) and (d), respectively. It is found that FET A shows much better linearity. More specifically, when the overdrive voltage $(V_{GS} - V_{\mathrm{TH}})$ is 0.45 V onward, the drain current almost perfectly matches the linear fit. To evaluate its nonlinearity of FET A, the deviation from the linear fit is derived, as shown in Fig. 1(c) after normalization to drain current. The deviation is below 1% in the measured range where overdrive voltage is greater than 0.5 V, showing an extremely low nonlinearity. In contrast, the I_D–V_G relation of FET B becomes totally parabolic, as shown

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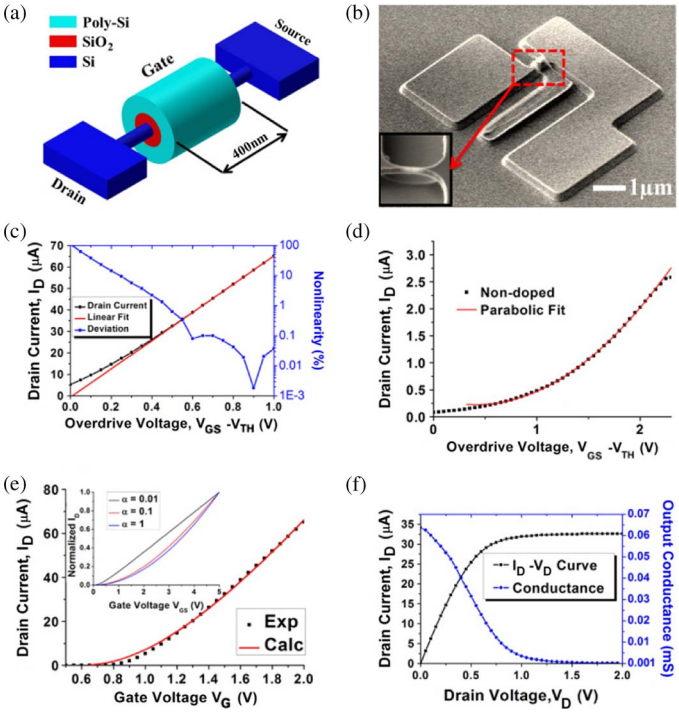

Fig. 1. (a) Schematic and (b) Scanning electron microscope (SEM) photos of the SiNW FET. (c) Transfer characteristic of FET A and its nonlinearity. (d) Transfer characteristics of FET B. (e) Calculated and measured I_D–V_G relations of FET A and (inset) I_D–V_G relations with different α values. (f) Output conductance of FET A.

in Fig. 1(d), which agrees well with the well-known square law. The square law is restated for the SiNW FET as follows:

$$I_{\mathrm{Dsat}} = \frac{2\pi\varepsilon_{\mathrm{ox}}}{\ln\left(\frac{R_{\mathrm{ins}}}{R_{\mathrm{wire}}}\right)} \cdot \frac{\mu}{L} \cdot (V_{GS} - V_{\mathrm{TH}})^2 \tag{1}$$

where μ is the mobility, $\varepsilon_{\mathrm{ox}}$ is the SiO_2 permittivity, L is the length of the SiNW, R_{wire} is the radius of the SiNW excluding SiO_2, and $R_{\mathrm{ins}} = R_{\mathrm{wire}} + t_{\mathrm{ox}}$ refers to the radius of SiNW including SiO_2. This result indicates that the linearity of the SiNW FET is highly dependent on the doping level. It is worth noting that the linear behavior of FET A seems to be like that of a short-channel MOSFET [4]. However, this linear behavior is mainly due to the carrier velocity saturation induced by high lateral electric fields within the short channel. Since FETs A and B have the same channel length but totally different linearities, the mechanism of FET A's linear behavior may differ from that of a short-channel MOSFET. Self-heating is another concern at such small scale and is suspected to contribute to the linear behavior as well. However, based on our simulation, the temperature of the inner SiNW is raised by only 13.5 K when it is under 50-μA bias. Under the high doping level, additional intrinsic carriers excited by self-heating are neglectable, and the mobility change is quite limited as well. Self-heating, therefore, may not be the major contributing factor to the linear behavior.

To investigate the mechanism of the SiNW FET's linear behavior, a theoretical model is adopted [5]. Saturation or turn-on current can be expressed as

$$I_{\mathrm{Dsat}} = \frac{\alpha}{(2\alpha - 1)} \frac{C_G}{L} \mu V_C \left[\alpha V_{\mathrm{GT}} - (s - \alpha) V_C\right] \tag{2}$$

$$s = \sqrt{\left(\alpha + (1-\alpha)\frac{V_{\mathrm{GT}}}{V_C}\right)^2 + 2\alpha(2\alpha - 1)\frac{V_{\mathrm{GT}}}{V_C}} \tag{3}$$

where C_G is the gate capacitance per unit length, $V_c = v_{\mathrm{sat}} \times L/\mu$ is the critical voltage, and $V_{\mathrm{GT}} = V_{GS} - V_{\mathrm{TH}}$ is the overdrive voltage. Tan *et al.* believed that the carrier velocity at the drain end may not be able to reach the ultimate saturation velocity due to the finite electric field. Parameter $\alpha = v_D/v_{\mathrm{sat}}$ is introduced, which is the fraction of saturation velocity that appeared at the drain. If $\alpha = 1$, (2) and (3) reduces to the most widely utilized standard form [5], [6]. This critical parameter is given by

$$\alpha = \frac{E_D/E_C}{1 + E_D/E_C} \tag{4}$$

where $E_D = V_{\mathrm{Dsat}}/\alpha L$, and $E_c = v_{\mathrm{sat}}/\mu$. Since FET A is degenerately doped, the mobility will be drastically degraded due to impurities scattering, and it is reasonable to choose 90 $\mathrm{cm}^2/\mathrm{V} \times \mathrm{s}$ for FET A. The saturation velocity will be up to 5×10^7 cm/s under such doping level [6]. Thus, the critical voltage V_c is obtained as 22 V for FET A. Normalized I_{Dsat} with selected $\alpha = 0.01$, 0.1, and 1, and $V_c = 22$ V are calculated, shown in the inset in Fig. 1(e). The I_D–V_G curve with $\alpha = 1$ is totally parabolic, whereas the curve with $\alpha = 0.01$ is almost totally linear. α determines the linearity of the SiNW FET, and smaller α means better linearity. Compared with FET B, degenerately doped FET A gives lower mobility and higher ultimate saturation velocity. According to (4), α for FET A is smaller, and thus, it should have higher linearity. This is consistent with the measured results as well. With V_c, v_{sat}, and μ for FET A previously discussed, the calculated I_D–V_G curve based on (2)–(4) is obtained in Fig. 1(e), which agrees well with the experimental data. With the help of the short-channel effect, the linearity would be even better if L is further reduced to sub-100 nm according to calculation. Fabrication and studies on such devices will be left as our future work.

Output conductance is another significant nonlinear source. In practice, the output conductance can never be zero, and the saturation current of a long-channel MOSFET can slightly increase with the drain voltage due to the channel-length modulation (CLM) effect. In terms of the short-channel MOSFET, it may be even worse as the drain-induced barrier lowering (DIBL) effect will result in a large output conductance. As the channel length scales down, the source and the drain may be eventually punched through, which will result in an extremely large output conductance [4]. Fortunately, the SiNW FET is immune from both of these side effects. The I_D–V_D curve and the output conductance of FET A at $V_{GS} = 1.5$ V are demonstrated in Fig. 1(f). When the drain current enters the saturation region, there is no further significant increment, and the output conductance is even down to nearly zero. Such low output conductance is because the SiNW FET employed a JL structure and, hence, there is totally no space charge region inside the SiNW FET. Thus, the source and the drain can never be punched through. In addition, the pinchoff effect is absent for FET A because the drain velocity can only be a fraction of the ultimate saturation velocity. The carrier concentration at the drain end can thus never drop to zero, which is also coherent to the current continuity at both drain and source ends of the

channel. The nonexistence of the pinchoff effect indicates that the channel length is independent of the drain voltage. Without suffering from the CLM and the DIBL, FET A exhibits a nearly ideal output conductance compared with both long- and short-channel MOSFETs. However, the output conductance of FET A is still a nonzero value, which is at the range of microsiemens. The saturation current does increase with the drain voltage beyond V_{Dsat}. α as the fraction of saturation velocity will be slightly raised by a higher electric field, implying a higher velocity at the drain end [5]. This velocity overshoot is not very crucial but will definitely cause the observed finite output resistance.

III. RF Applications and Conclusion

For RF applications, generally, some components, which are not harmonics of the input frequencies, will be added to output signals, if two different frequencies signals are applied to a nonlinear system. This phenomenon is called the IM, resulting from nonlinear mixing or multiplication [1]. The IM is troublesome in an RF system because the IM products of two nearby interfering signals outside the band of interest may fall into it, corrupting the desired signals. Among all IMs, the third-order IM (IM3) is the most commonly faced and most critical. The third-order intercept point (IP3) of the gate voltage amplitude is the most widely used one to criticize this kind of nonlinear distortion [1].

However, this model is too simple, which only considers the nonlinearity from transconductance; thus, it is not suitable for the SiNW FET's linearity analysis. Kang *et al.* proposed another model for analysis, which takes the effects of both transconductance and output conductance into account and is more accurate than the simple IP3 model [2]. In this model, the IM3 currents are calculated to reflect the distortion level. By taking a 0.25 μm $\times$ 10 μm $\times$ 10 NMOS made by the Taiwan Semiconductor Manufacturing Company (TSMC) Ltd., Taiwan, as a reference [2], the output IM3 currents at various load resistances of FET A are calculated, which are biased at $V_{DS} = 1.5$ V and $V_{GS} = 1.4$ V to ensure the same overdrive voltage with the TSMC one, as shown in Fig. 2(a)–(c). It is worth noting that both the gate length and the gate thickness of the TSMC NMOS are not the same as those of FET A and their total output currents are different as well. To conduct a fair comparison, all IM3 currents are normalized with respect to the total output currents, and the corresponding IM3 current percentages in total output currents are compared.

Transconductance is the dominant nonlinear source at low load resistances, while nonlinearity from output conductance dominates at high load resistances. Benefiting from the linear I_D–V_G relation as previously discussed, modern short-channel MOSFET shows a low IM3 current at low load resistances. However, FET A performs even better than its counterpart with a -6-dB lower IM3 current at 10-Ω load resistance. When the load resistance goes beyond 100 Ω, the nonlinearity of the MOSFET dramatically increases because of its serious short-channel effects. Unfortunately, load resistances within this range are most commonly utilized, and under such cases, systems built with short-channel MOSFETs will suffer from significant IM distortions. On the contrast, since FET A is immune to both CLM and DIBL as previously discussed, its IM3 current from the output conductance can be totally neglected.

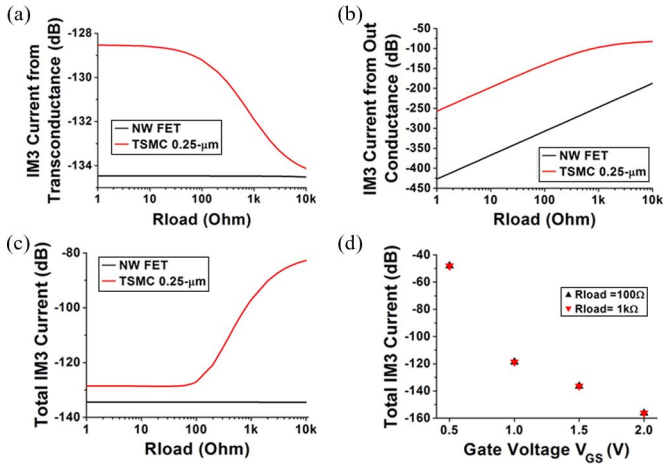

Fig. 2. Output IM3 current of FET A and TSMC 0.25-μm short-channel MOSFET in 20log scale. (a) IM3 from transconductance. (b) IM3 from output conductance. (c) IM3 from both transconductance and output conductance. (d) Total IM3 currents under different V_{GS} values.

No significant change of IM3 current with the load resistance can be observed for FET A, indicating its perfectly low and stable nonlinearity.

Total IM3 currents under different V_{GS} values with a fixed drain voltage of 1.5 V are also shown in Fig. 2(d). The load resistance seems not to influence the nonlinearity much. When FET A is turned on, the total IM3 current will decrease with the gate voltage, showing an increasing linearity. This trend is coherent with previous results in Fig. 1(c). We further compare the highest total IM3 current of FET A at the threshold voltage $V_{GS} = 1$ V with the TSMC counterpart; it is still -21 dB better than the TSMC one for 1-kΩ load resistance. With the employment of the SiNW FET, a simple and low-cost RF system with low distortions may be possible. Specially designed stages and blocks will no longer be necessary to achieve a high linear performance.

In conclusion, n-type GAA JL SiNW FETs have been developed and characterized, of which the degenerately doped one shows an extremely high linearity. Due to its degenerate doping level and JL structures, nonlinearities from both transconductance and output conductance have been minimized. Its linear performance for the RF application is much better than a modern short-channel MOSFET. It is of great potential in applications that demand high linearity.

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