AIP | Applied Physics Letters

A bi-stable nanoelectromechanical non-volatile memory based on van der Waals force

Bo Woon Soon, Eldwin Jiaqiang Ng, You Qian, Navab Singh, Minglin Julius Tsai et al.

Citation: Appl. Phys. Lett. **103**, 053122 (2013); doi: 10.1063/1.4817796
View online: http://dx.doi.org/10.1063/1.4817796
View Table of Contents: http://apl.aip.org/resource/1/APPLAB/v103/i5
Published by the AIP Publishing LLC.

A bi-stable nanoelectromechanical non-volatile memory based on van der Waals force

Bo Woon Soon,[1,2,a)] Eldwin Jiaqiang Ng,[3] You Qian,[1,2] Navab Singh,[1] Minglin Julius Tsai,[1,b)] and Chengkuo Lee[2,a)]
[1]*Institute of Microelectronics, Agency for Science, Technology and Research (A*STAR), 11 Science Park Road, Singapore Science Park II, Singapore 117685*
[2]*Department of Electrical and Computer Engineering, National University of Singapore, 4 Engineering Drive 3, Singapore 117576*
[3]*Department of Mechanical Engineering, Stanford University, 440 Escondido Mall, Bldg 530-224 Stanford, California 94305, USA*

(Received 28 March 2013; accepted 17 July 2013; published online 2 August 2013)

By using complementary-metal-oxide-semiconductor processes, a silicon based bi-stable nanoelectromechanical non-volatile memory is fabricated and characterized. The main feature of this device is an 80 nm wide and 3 μm high silicon nanofin (SiNF) of a high aspect ratio (1:35). The switching mechanism is realized by electrostatic actuation between two lateral electrodes, i.e., terminals. Bi-stable hysteresis behavior is demonstrated when the SiNF maintains its contact to one of the two terminals by leveraging on van der Waals force even after voltage bias is turned off. The compelling results indicate that this design is promising for realization of high density non-volatile memory application due to its nano-scale footprint and zero on-hold power consumption.
 [http://dx.doi.org/10.1063/1.4817796]

At present, demonstration of complementary-metal-oxide-semiconductor (CMOS) processes based non-volatile semiconductor memory devices, especially using the floating gate designs, has nourished several kinds of memory ranging from EEPROM to the prominent Flash memory.[1–3] In order to pursuit enhancement in performance and cost, devices are continuously scaled, and power handling issue becomes a major concern due to subthreshold leakage, lowering of threshold voltage (Vth), and relatively high drain voltage (Vdd).[4–6] This results in extensive research in memory technology such as magnetoresistive random access memory (MRAM), ferroelectric random access memory (FERAM), silicon-oxide-nitride-oxide-silicon memory (SONOS), and resistive random access memory (ReRAM) in pursuance of succession candidate to the current reigning NAND and NOR Flash technology.[7–12] Although nanoelectromechanical systems (NEMS) switches have been investigated and reported as one of the solutions to next-generation IC technology in parallel to CMOS scaling,[13–16] it is more important to note that application of NEMS switches in memory designs is able to achieve efficient power consumption and faster erasing speed.[17–19] Advantages of NEMS switches includes ideal zero off-state current, steep sub-threshold slopes, lower power, and capability in high temperature application.[20–24] Incorporation of NEMS switches in conventional CMOS circuits also known as hybrid CMOS-NEMS has been discussed and reported, where delay reduction and faster erasing operation are demonstrated by stacking the NEMS relay on top of CMOS circuits or utilizing NEMS switch for storage layer discharging.[25–28] Notably, NEMS switches made from different materials such as carbon nanotubes (CNTs), diamond, and silicon carbide (SiC) have been demonstrated with promising results.[29–32] However, most reported devices above only demonstrate transistor switching on-off operation, but are not capable of operating as non-volatile memory (NVM). Furthermore, the growth and assembly of these materials such as CNTs are challenging to be realized in mass production.[33,34] In order to design a power efficient NEMS memory with low voltage operating condition, a nanoscale laterally movable silicon nanofin (SiNF) is proposed. The switch relies on adhesion between contacts to realize bi-stable states, resulting in a hysteresis curve which operates like a non-volatile memory. Usually adhesion is a failure mode that causes permanent stiction for most microelectromechanical systems (MEMS), but in present case, it turns out to be an advantage because we can leverage on adhesion to keep the SiNF at its last actuated position such that there is no on-hold power consumption. Besides, we present the optimization effort in the complementary two lateral terminals design in order to achieve bi-stable hysteresis property. With this property, the proposed NEMS memory is a storage-layer-free NVM.

The schematics diagram of the NEMS NVM is shown in Fig. 1(a). SiNF NEMS devices with dimension of 80 nm (h) × 3 μm (d) × various lengths (l) of 2, 8, and 12 μm situated between two anchored terminals are fabricated and characterized. The SiNF is actuated electrostatically to contact one of the two terminals when operation voltage is applied between the SiNF and either terminal. After the SiNF switched to one terminal, the bias voltage is turned off and the SiNF maintains its contact with this terminal due to adhesion between the surfaces of the silicon fin and electrode terminal. When the electrostatic potential is gradually increased at the opposite terminal, the fin flips and switches towards the opposite lateral terminal. The entire loop forms a hysteresis curve identical to non-volatile operation

[a)]Authors to whom correspondence should be addressed. Electronic addresses: soonbw@ime.a-star.edu.sg and elelc@nus.edu.sg
[b)]Present address: Invensense, Inc., 1197 Borregas Avenue, Sunnyvale, California 94089, USA.

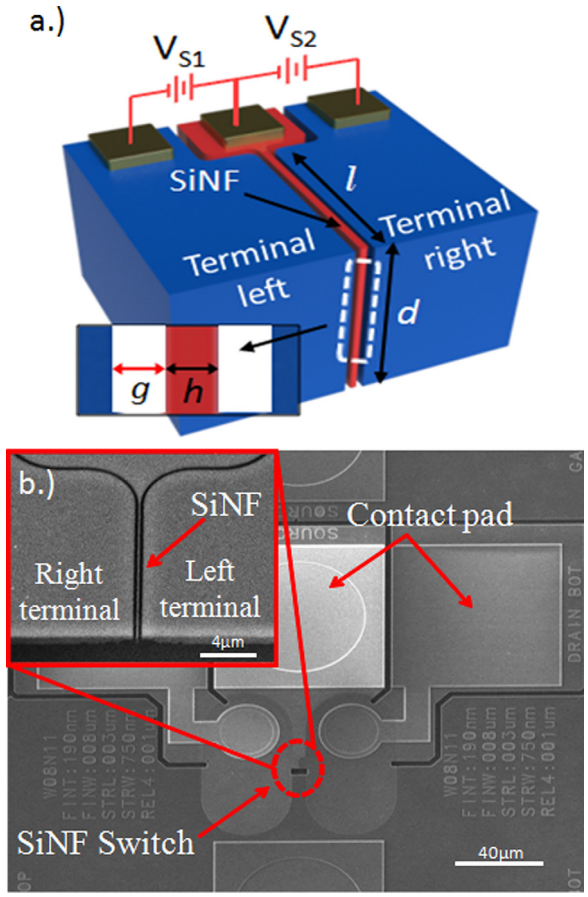

FIG. 1. (a) 3D schematic of the NEMS memory with SiNF as the actuator that can switch between two terminals. (b) SEM image of a 12 μm long memory device with contact pads and the location of the SiNF. Inset: Zoomed in image of the SiNF after HF vapor release.

showing that SiNF can be applied in NVM application. In order to achieve this, high aspect ratio dimension is necessary for the van der Waals (VDW) force to overcome the spring restoring force for it to maintain the contact in position. Meanwhile, the width of the SiNF has to be nano-scale in order to minimize the SiNF's length. The characterization shows a 2 μm SiNF based NVM is achievable.

The fabrication process of the SiNF based NVM begins with a silicon-on-insulator (SOI) wafer which has 3 μm device layer and 1 μm buried oxide layer (BOX). The scanning electron microscopy (SEM) photos of SiNF structure in bird's eye view with respect to various steps in the process flow are shown in Fig. 2. A 300 nm SiO_2 layer is deposited and patterned as a hardmask for the deep reactive ion etching (DRIE) to etch the Si device layer in order to define the SiNF. An optimized DRIE recipe is used to reduce the scallop shape of the etched Si sidewall while keeping it vertical, i.e., 90°. The aspect ratio of the etch SiNF is measured as 1:17. After that, 1100 °C dry oxidation is processed to trim down the SiNF thickness to the final target of 80 nm; the additional oxidation is required to make the SiNF thinner to achieve final aspect ratio of 1:35, and simultaneously the oxidation reduces surface roughness of the etched sidewall to further enhance the van der Waals adhesion. The grown SiO_2 during the oxidation is later removed by diluted wet hydrofluoric (HF) acids. Next another layer of 80 nm conformal SiO_2 is deposited by low pressure chemical vapor deposition (LPCVD) and later is sacrificially etched to form the nanogap (g) between the SiNF and the lateral terminals. This is done selectively using a photoresist mask. After that, thick polycrystalline silicon is filled as the terminals and chemical mechanical polishing is used to flatten the entire wafer while separating both SiNF and the two terminals. A layer of dielectric is deposited to isolate the electrical interconnects, and bond pad is formed with aluminum metallization so that the device can be tested conveniently using probe station. A final isolation trench is patterned and etched to isolate the terminals as well as forming the release hole to release the SiNF. After isolation trench, the SiNF is finally released in HF acid vapor, since the SiNF is fabricated from the device layer, the SiNF is stress free and we found that the SiNFs remain straight in neutral position when they are first released. Both the device layer and the polycrystalline silicon back filled are heavily implanted twice with 5×10^{15} ions/cm^2 Arsenic dopant and activated with high temperature of 1050 °C for 12 h. Fig. 1(b) shows the SEM image of a 12 μm SiNF device where contact pads are metalized. The metallization is isolated with a layer of thick

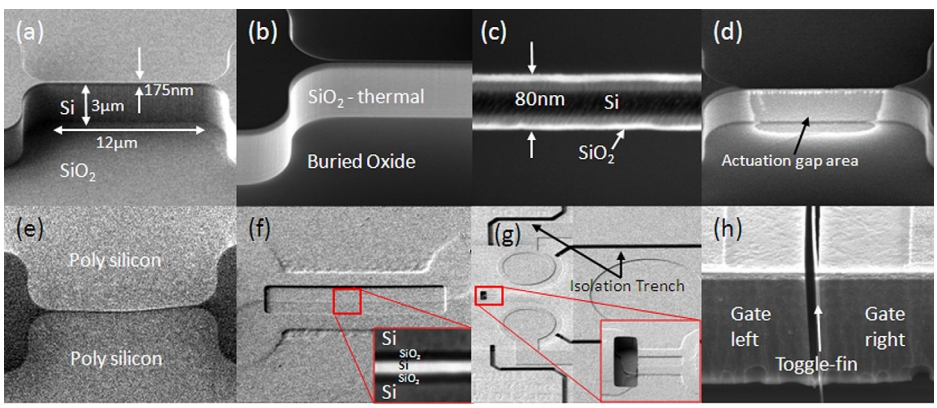

FIG. 2. SEM pictures of the toggle-fin fabrication process flow. (a) High aspect ratio silicon fin etch of 1:17. (b) Further oxidation to thin down the fin width to approximately aspect ratio of 1:35 (80 nm), at the same time smoothing the silicon's surface. (c) Removal of SiO_2 with HF acids around the fin. (d) LPCVD of SiO_2 dielectric for insulation for overall area followed by reduction etch using HF acids around the fin area to create 80 nm gap for electrostatic actuation. (e) Top view after thick polycrystalline silicon deposition followed by planarization until toggle-fin surface. (f) Dielectric deposition for insulation of metallization. This layer is opened at the toggle-fin area so that the release etching is possible. (Inset) Top scan shows silicon fin, silicon gate electrodes, and sacrificial SiO_2 layers. (g) Isolation trench stop on BOX to isolate the toggle-fin and the gate-electrodes. (Inset) Etching of release hole. (h) Release etching of toggle-fin using hydrofluoric acid vapor (VHF).

dielectric layer so that it will survive the HF vapor etching during the release. A zoom-in image of the SiNF shows that the SiNF is straight and does not suffer from any bending due to stress and all SiNF are at neutral position.

The fabricated devices are tested under N_2 purge environment in CASCADE microchamber (RBL-6100) at 50 °C. The testing starts 30 min after the temperature reached its setting temperature. This procedure is performed to remove the moisture in the chamber so that capillary force is assumed negligible. Voltage sweep is applied across the SiNF to one of the terminal and return to zero; this step is repeated vice versa to another terminal. In a switch testing, an abrupt increase in current depicts the SiNF contact to the terminal. In order to achieve a NVM, the SiNF has to be kept in contact by van der Waals force even when the voltage sweep returns to zero. This criterion is met as there is no pull-out or abrupt current drop detected as the voltage sweep to zero. Fig. 3 shows the I-V characteristics of 2 μm and 8 μm SiNF, respectively. From both measurements, the initial pull-in voltage (V_{PI}) of the device is lower compared to the rest of the resetting voltage (V_{RESET}); this is due to the initial neutral position of the SiNF, where the gap is approximately 80 nm. After the first pull-in, the subsequent operation voltage will be V_{RESET} where the largest gap can be 160 nm maximum at the tip. Thus, larger electrostatic force

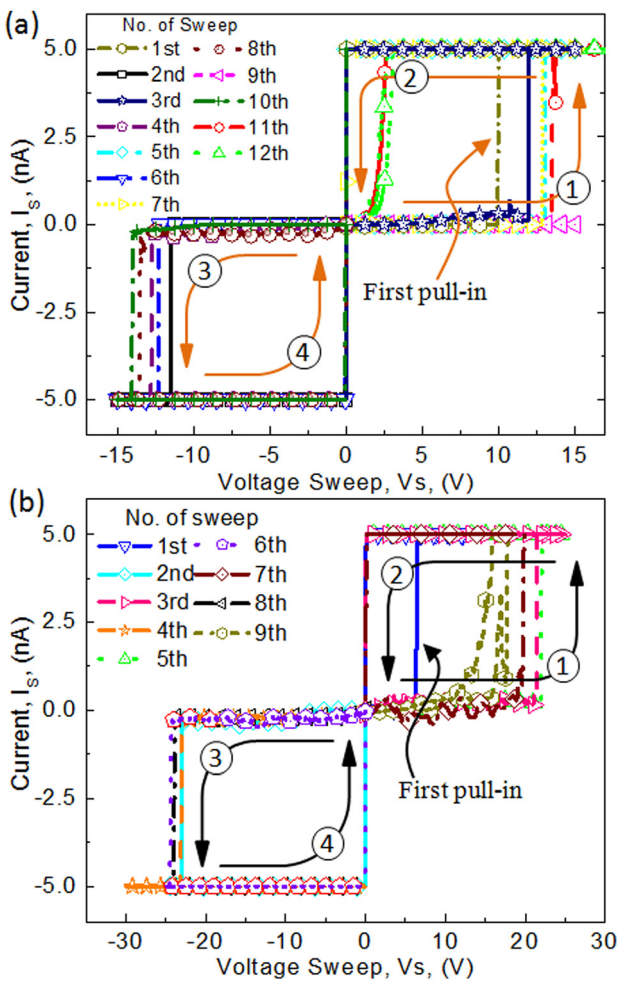

FIG. 3. Bi-stable I-V characteristic of the NEMS memory. (a) 2 μm SiNF device (b) 8 μm SiNF device. Note that the current in continuous when voltage sweep returns to 0 V.

is required to reset the switch. The sequence of the hysteresis comes about in a sequence from 1 to 4. In sequence 1, the SiNF is pull-in to the right terminal, when the voltage sweep returns to zero in sequence 2, no pull-out is detected depicting that the SiNF is still in contact with the right terminal. As the voltage sweep across the opposite terminal in sequence 3, the SiNF flips as $F_{ELECTROSTATIC} + F_{SPRING} > F_{VDW}$. As the voltage sweep returns to zero in sequence 4, van der Waals force again holds the SiNF in contacts, as $F_{VDW} > F_{SPRING}$. Altogether, the device demonstrated a bi-stable hysteresis curve, thus, the device operates like a NVM. The 2 μm SiNF operates for the 11th sweep before failing as current returns to zero during voltage back sweep resembling a discharging curve at around 3–4 V, following 12th sweep traces the same charging curve as voltage sweep vice versa. The same phenomenon happens at the 9th sweep of the 8 μm SiNF device. The devices are inspected under SEM and it is found that the SiNF has burnt and melted to either terminal. It is known that joule heating can be detrimental to such devices. However, there is possibility of utilizing high melting point material like SiC, or tungsten, in order to improve the reliability of switching.[32] It is also reported that metal coating such as platinum or gold may enhance the reliability of the switching and reduces contact resistance.[35,36]

In contrast, we also notice that all 12 μm device can only be activated once and no V_{RESET} can be detected anymore until the switching voltage reaches breakdown at approximately 120 V. It is interesting to note that these devices can be actuated under the charging of SEM. We deduced that the actuation is highly depending on the electron beam scanning and it happens more often during higher magnification. Fig. 4 shows the SEM images of all three SiNF devices, which is actuated under the SEM. After SEM, this device is measured and we found that the switching direction is consistent with the SEM inspection. From these images, the contact area can be extracted. 12 μm devices have the largest contact area, the first pull-in contact of such device is catastrophic and causes the device to fail due to permanent adhesion. From the result, we know that van der Waals adhesion cannot be too strong compared to the spring restoring force in order to enable a re-writeable NVM. The spring restoring force and van der Waals force can be determined using respective model[37–39] and the force versus measured adhesion area is shown in Fig. 5. The spring restoration force equation is shown as follows:

$$F_{spring} = \frac{E}{(1-v^2)} \times \frac{dh^3}{4l^3} \times g, \tag{1}$$

where E is the Young's modulus; υ is the passion ratio; and d, h, and l are the depth, thickness, and length of the SiNF, respectively. Meanwhile, the van der Waals force equation according to the Lennard Jones potential, which is shown below

$$F_{VDW}(per\ unit\ area) = \frac{A_H}{6\pi} \times \left[\frac{1}{g_o} - \frac{{r_o}^6}{{g_o}^9}\right], \tag{2}$$

where A_H is the Hamaker's constant, r_o is the interatomic equilibrium distance, and g_o is the cut-off distance when the

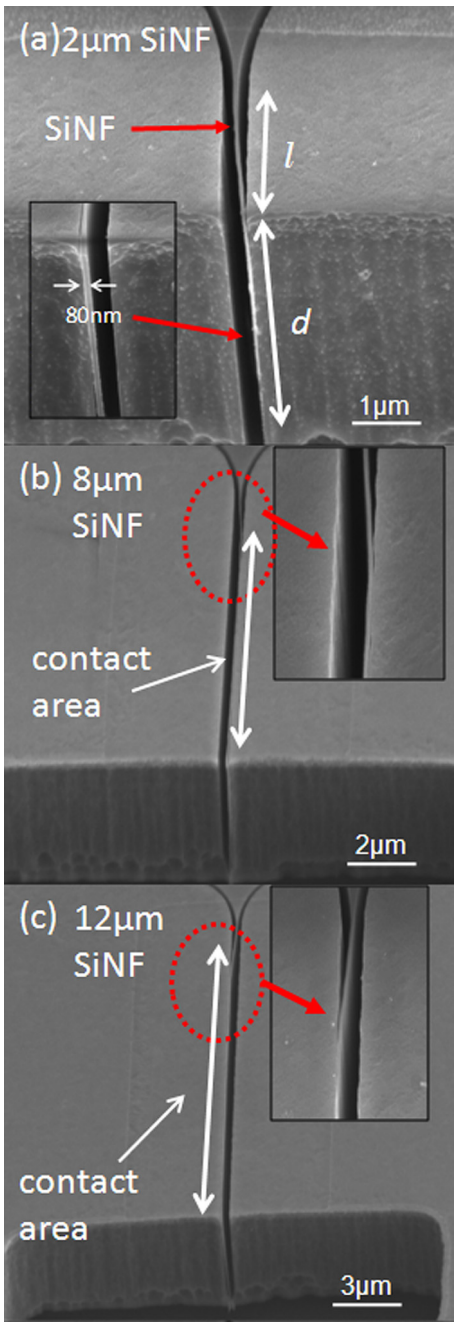

FIG. 4. SEM images of SiNF. (a) 2 μm SiNF. Inset: Zoomed in of contact between SiNF and terminal. (b) and (c) 8 and 12 μm SiNF devices. Insets: Zoom in view of SiNF bending and in contact with either terminal.

SiNF is in contact. Reported Hamaker's constant of Si and SiO_2 is used.[40] However, the total adhesion force is highly experimental and commonly can be extracted with AFM experiment.[41] Therefore, it is assumed VDW adhesion is predominant in closed gap in order to simplify the model for ease of deciding experimental parameters. While the cantilever structure of the device is simplest and can be physically scaled using state-of-the-art equipment, we found that the area of adhesion is critical since it is proportional to the length and width of the SiNF. The aspect ratio of length and thickness of the SiNF is approximately at 1:25, so that that VDW force can overcome the spring force. To further scale this, the rule of thumb for the cantilever to become non-volatile, for instance, a 10 nm thick $\times$ 250 nm length SiNF is

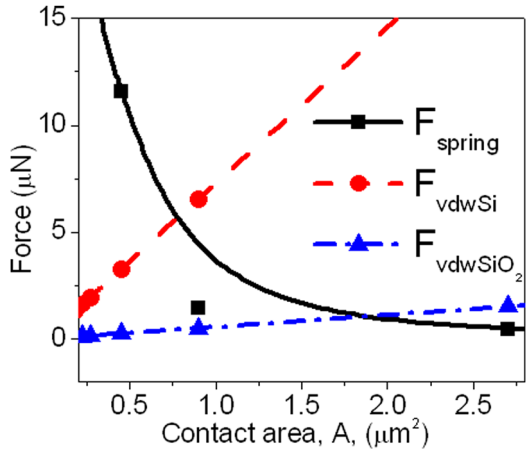

FIG. 5. Spring and van der Waals forces of silicon beam versus measured contact area of SiNF for both contact surfaces of Si and SiO_2.

adequate. Native SiO_2 on the surface of the polycrystalline silicon is assumed to be negligible in terms of mechanical switching characteristics, but it is important to compare this phenomenon, under VDW operation. Referring to Fig. 4, it is significant to analyze the exponential decaying spring restoration force, F_{SPRING} versus the linear VDW force, F_{VDW} of Si and SiO_2. In order to design a NVM, SiNF length corresponds to effective area where F_{VDW} is higher than F_{SPRING} is preferred. Nonetheless, if the SiNF is too long, this will cause a large area of contact, resulting in a non-resettable switch. From the results, we found that 2 μm length is optimum where contact area is minute and the switch is resettable. Although native SiO_2, approximately in 10 Å, can grow on the Si surface after releasing the SiNF, the result shows that F_{VDW} on Si surface seems to agree with the experiment, depicting that native oxide is possibly negligible in this device. To further confirm this, we found that after actuating the SiNF to either terminal, the contact between the two terminals is ohmic after repeating a low voltage sweep on the actuated SiNF adhered to either terminal at low current compliance of 50 nA. This is probably due to the large electrostatic force which is able to break through the native oxide layer and form better electrical contact with the Si surface, and there is no sign of charging effect. Meanwhile, the result agrees well with the experimental observation where the 2 μm devices with very little contact area were able to hold the SiNF in contact. To further improve the pull-in voltage, one possible approach is to leverage on torsional devices so that the spring constant relies on the torsion anchor instead of the beam length. In this way, the device contact area is more flexible and lower operating voltage can be achieved.[42,43] In order to find out temperature dependency of the pull-in voltage, pull-in voltage of different SiNF lengths at elevated temperature measured. Overall, the device has low mean voltage drift of 24 mV/K.[44] Pull-in voltage of three SiNF with 2, 8, and 12 μm is experimentally tested at 50, 100, and 150 °C, which is maximum temperature limit of our testing facility.

In conclusion, we have reported a bi-stable non-volatile memory based on van der Waals force. This device relies on a high aspect ratio SiNF that switch and latch between two permanent terminals. The nanoscale footprint of this device

is favorable towards power efficient application in NVM. Besides that, it is possible to design a storage layer free NVM which can complement the current CMOS driving circuit to improve the erasing cycle comparing to state of the art Flash memory. The fabrication of this device is CMOS compatible, and bi-stable hysteresis curve is characterized on a SiNF device based on VDW force. However, further investigation on contact material is necessary to improve the device performance.

The author would like to thank Dr. Vincent Pott for valuable discussion. This work was supported by the Science and Engineering Research Council (SERC), Agency for Science, Technology and Research (A*STAR), Singapore, under Grant Nos. 102-101-0022 and 102-165-0084.

[1]C. H. Lee, S. H. Hur, Y. C. Shin, J. H. Choi, D. G. Park, and K. Kim, Appl. Phys. Lett. **86**, 152908 (2005).
[2]B. Roberto, E. Camerlenghi, A. Modelli, and A. Visconti, Proc. IEEE **91**(4), 489–502 (2003).
[3]P. Pavan, R. Bez, P. Olivo, and E. Zanoni, Proc. IEEE **85**(8), 1248–1271 (1997).
[4]Y. Taur, IBM J. Res. Dev. **46**(2/3), 213–222 (2002).
[5]L. Chang, D. M. Fried, J. Hergenrother, J. W. Sleight, R. H. Dennard, R. K. Montoye, L. Sekaric, S. J. McNab, A. W. Topol, C. D. Adams, K. W. Guarini, and W. Haensch, Dig. Tech. Pap. - Symp. VLSI Technol. **2005**, 128–129.
[6]C. Ching-Te, S. Mukhopadhyay, J. J. Kim, K. Kim, and R. Rao, in *IEEE International Workshop on Memory Technology, Design and Testing* (2007), pp. 4–12.
[7]S. Tehrani, J. Slaughter, M. Deherrera, B. N. Engel, N. D. Rizzo, J. Salter, and G. Grynkewich, Proc. IEEE **91**(5), 703–714 (2003).
[8]J. Bu and M. H. White, Solid-State Electron. **45**(1), 113–120 (2001).
[9]S. E. Ahn, M. J. Lee, Y. Park, B. S. Kang, C. B. Lee, K. H. Kim, and B. H. Park, Adv. Mater. **20**(5), 924–928 (2008).
[10]K. Kim and Y. J. Song, Microelectron. Reliab. **43**(3), 385–398 (2003).
[11]R. Waser and M. Aono, Nature Mater. **6**(11), 833–840 (2007).
[12]R. Waser, R. Dittmann, G. Staikov, and K. Szot, Adv. Mater. **21**(25–26), 2632–2663 (2009).
[13]Y. Qian, L. Lou, M. J. Tsai, and C. Lee, Appl. Phys. Lett. **100**(11), 113102 (2012).
[14]K. Akarvardar, D. Elata, R. Parsa, G. C. Wan, K. Yoo, J. Provine, P. Peumans, R. T. Howe, and H. S. P. Wong, Tech. Dig. - Int. Electron Devices Meet. **2007**, 299–302.
[15]J. O. Lee, Y. H. Song, M. W. Kim, M. H. Kang, J. S. Oh, H. H. Yang, and J. B. Yoon, Nat. Nanotechnol. **8**, 36–40 (2012).
[16]F. K. Chowdhury, D. Saab, and M. Tabib-Azar, Sens. Actuators, A **188**, 481–488 (2012).
[17]W. W. Jang, J. Lee, J. Yoon, M. Kim, J. Lee, S. Kim, K. Cho, D. Kim, D. Park, and W. Lee, Appl. Phys. Lett. **92**(10), 103110 (2008).
[18]J. P. Hollingsworth and P. R. Bandaru, Appl. Phys. Lett. **87**(23), 233115 (2005).
[19]J. M. Kinaret, T. Nord, and S. Viefers, Appl. Phys. Lett. **82**(8), 1287–1289 (2003).
[20]O. Y. Loh and H. D. Espinosa, Nat. Nanotechnol. **7**, 283–295 (2012).
[21]F. Chen, H. Kam, D. Markovic, T. K. Liu, V. Stojanovic, and E. Alon, in *ICCAD Proceedings* (2008), pp. 750–757.
[22]Y. T. Yang, K. Ekinci, X. M. H. Huang, L. M. Schiavone, M. L. Roukes, C. A. Zorman, and M. Mehregany, Appl. Phys. Lett. **78**(2), 162–164 (2001).
[23]J. E. Jang, S. N. Cha, Y. Choi, G. A. Amaratunga, D. J. Kang, D. G. Hasko, and J. M. Kim, Appl. Phys. Lett. **87**(16), 163114 (2005).
[24]V. Joshi, C. Khieu, C. G. Smith, C. Schepens, F. Csaszar, D. Lacey, T. Nagata, M. Renault, R. Van Kampen, R. Knipe, and D. Yost, in *Interconnect Technology Conference* (2010), pp. 1–3.
[25]S. W. Lee, S. J. Park, E. E. B. Campbell, and D. Chen, Nat. Commun. **2**, 220 (2011).
[26]C. Dong, C. Chen, S. Mitra, and D. Chen, in *13th IEEE International Workshop* (2011), pp. 1–8.
[27]H. You and W. Cho, Appl. Phys. Lett. **96**(9), 093506 (2010).
[28]S. Chong, K. Akarvardar, R. Parsa, J. B. Yoon, R. T. Howe, S. Mitra, and H. S. P. Wong, in *IEEE/ACM International Conference on Computer-Aided Design* (2009), pp. 478–484.
[29]A. B. Kaul, E. W. Wong, L. Epp, and B. D. Hunt, Nano Lett. **6**(5), 942–947 (2006).
[30]P. Schmid, F. J. Hernandez-Guillen, and E. Kohn, Diamond Relat. Mater. **12**(3), 418–421 (2003).
[31]M. Liao, Z. Rong, S. Hishita, M. Imura, S. Koizumi, and Y. Koide, Diamond Relat. Mater. **24**(7), 69–73 (2012).
[32]T. H. Lee, S. Bhunia, and M. Mehregany, Science **329**(5997), 1316–1318 (2010).
[33]P. L. McEuen, M. S. Fuhrer, and H. Park, IEEE Trans. Nanotechnol. **1**(1), 78–85 (2002).
[34]A. Javey, J. Guo, Q. Wang, M. Lundstrom, and H. Dai, Nature **424**(6949), 654–657 (2003).
[35]R. Parsa, M. Shavezipur, and W. S. Lee, in *IEEE 24th International Conference on Micro Electro Mechanical Systems (MEMS)* (2011), pp. 1361–1364.
[36]D. Lee, W. S. Lee, J. Provine, J.-O. Lee, J.-B. Yoon, R. T. Howe, S. Mitra, and H.-S. P. Wong, in *23rd IEEE Micro Electro Mechanical Systems Conference* (2010), pp. 24–28.
[37]A. Ramezani, A. Alasty, and J. Akbari, Microsyst. Technol. **12**(12), 1153–1161 (2006).
[38]V. Pott, G. L. Chua, R. Vaddi, J. L. Tsai, and T. T. Kim, IEEE Trans. Electron Devices **59**(4), 1137–1143 (2012).
[39]A. Hariri, J. W. Zu, and R. B. Mrad, J. Micromech. Microeng. **16**(7), 1195 (2006).
[40]J. Visser, Adv. Colloid Interface Sci. **3**(4), 331–363 (1972).
[41]F. W. DelRio, M. P. De Boer, J. A. Knapp, E. D. Reedy, Jr., P. J. Clews, and M. L. Dunn, Nature Mater. **4**, 629–634 (2005).
[42]W. Xiang and C. Lee, Appl. Phys. Lett. **96**(19), 193113 (2010).
[43]A. Gusso and G. J. Delben, Sens. Actuators, A **135**(2), 792–800 (2007).
[44]B. Soon, N. Singh, J. M. Tsai, and C. Lee, in *17th International Conference on Solid-State Sensors, Actuators and Microsystems, Transducers (Transducer' 13)* (2013), T2D.001.