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A dual-silicon-nanowires based U-shape nanoelectromechanical switch with low pull-in voltage

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A dual-silicon-nanowires based U-shape nanoelectromechanical switch with low pull-in voltage is fabricated using standard complementary metal-oxide-semiconductor compatible process on silicon-on-insulator wafer. The switch consists of a capacitive paddle with dimension of 2 μm by 4 μm supported by two silicon nanowires, suspended on top of the substrate with a gap of 145 nm. The nanowires are 5 μm long with cross-section of 90 nm by 90 nm. The average pull-in voltage is about 1.12 V and the ratio of the ON/OFF current is measured to be over 10 000. According to the preliminary results, this U-shape structure demonstrates great potential in lowering down the pull-in voltage. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.3693382]

During the past few decades, silicon based complementary metal-oxide-semiconductor (CMOS) technology has been continuously scaling down in order to achieve better performances and lower cost. However, the charge-based operating mechanisms of CMOS devices represent a thermodynamic limit.[1] High leakage current in the off state makes such CMOS devices difficult to be scaled down further. Meanwhile, nanoelectromechanical system (NEMS) switches have been demonstrated in areas such as radio frequency,[2] nonvolatile memory,[3] and logical devices,[4,5] which exhibit several advantages like negligible off current and abrupt switching. Although piezoelectric crystalline $Pb(Zr,Ti)O_3$ (PZT) thin film actuators have been reported to be operated at voltage less than 1 V,[6,7] PZT is not a CMOS material. Among the different actuation mechanisms which can be realized by CMOS process, electrostatic actuation is favored for its low power consumption and fast switching speed. The typical pull-in voltage is 5–30 V from the recent reports,[8–10] which makes it incompatible with the modern CMOS circuit. There are various approaches to deal with the high pull-in voltage issue and the most effective way is to scale down the dimension. Carbon based material have demonstrated its enormous potential on making extremely small devices.[11–13] Such excellent switching characteristics can be exemplified by using carbon nanotube (CNT) NEMS switches.[14] CNT based switches can be operated at 4.5 V.[15] However, the fabrication processes for CNT is not CMOS compatible and the variability on the CNT alignment and dimension hinder CNT NEMS switches from developing into a mass market product. In addition, CNT also grows into metallic or semiconductor material randomly by nature which makes the performance undetermined.

Silicon nanowire (SiNW) based devices have several great properties like giant piezoresistive[16] effect and it has also been proven in its potential as low pull-in voltage switches.[17] The scaling down of the dimension makes the nanowire easy to be actuated but also reduces the electrostatic force it received. In this paper, a dual-silicon-nanowires based U-shape CMOS-NEMS switch is designed and characterized to demonstrate its low actuation voltage. The fabricated NEMS switch shows remarkably low pull-in voltage and nearly zero off current, high ON/OFF current ratio and repeatable switching behavior in ambient air.

The schematic diagram of the NEMS switch is shown in Fig. 1(a). Two silicon nanowires are fixed in one end on top of the insulating layer and electrically connected by a metal contact. The other ends of the SiNWs are connected by a movable capacitive paddle to increase the electrostatic force. Therefore, the U-shape structure consists of one capacitive paddle supported by two SiNWs and suspended above the Si

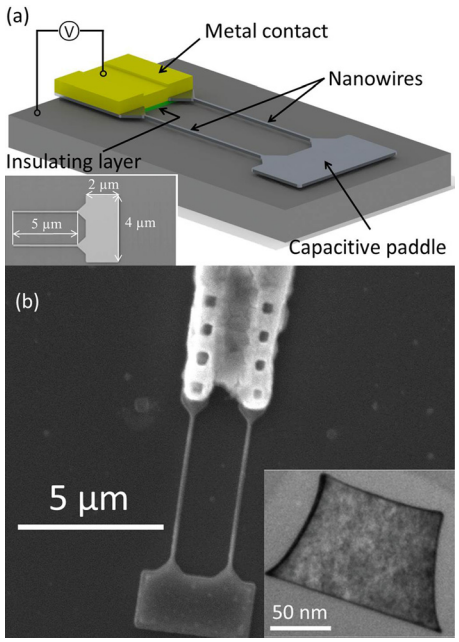

FIG. 1. (Color online) (a) A schematic illustration of the U-shape NEMS switch. (b) SEM photo of a U-shape NEMS switch after HF vapor releasing, Inset: TEM image of a SiNW cross-section.

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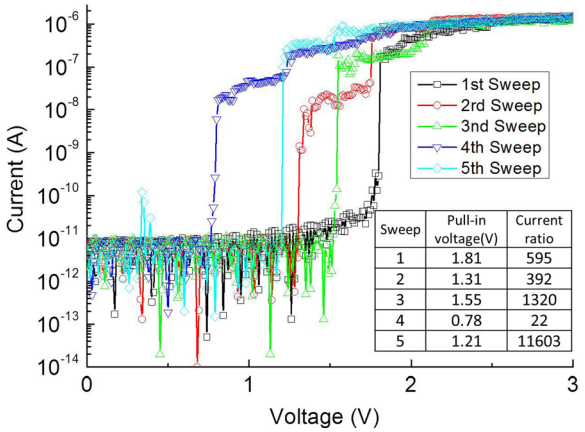
substrate. Both the SiNWs have equal lengths of 5 μm and are separated by 2 μm. The cross-section of the SiNW is nearly squarish, with side length of 90 nm. Once voltage is applied between the capacitive paddle and the substrate, the electrostatic force would bend the SiNWs down and make the capacitive paddle have an electrical contact with the substrate. The combination of large capacitive paddle and flexible SiNWs makes the U-shape structure bending more effectively under electrostatic actuation. The purpose of using two SiNWs is to provide a balanced spring restoring force for the capacitive paddle, avoiding torsion behavior happens in the SiNWs.

The fabrication process of the U-shape NEMS switch starts with a silicon-on-insulator (100) wafer, with device layer of 117 nm and buried oxide (BOX) layer of 145 nm. After the first photolithography, which defines the SiNWs and capacitive paddle, the photoresist is trimmed, and the critical dimension is decreased to around 100 nm. The SiNW is then patterned along (110) directions. To further shrink down the dimension of SiNW, thermal oxidation is conducted with the final cross section of the SiNW being 90 nm $\times$ 90 nm (Fig. 1(b)). The capacitive paddle is also oxidized on top and has a thickness of 90 nm. To increase the conductivity of SiNW and capacitive paddle, a p-type implantation process using BF_2+ with a dosage of 1×10^{14} ion/cm^2 is done, followed by annealing for dopant activation. Measurement result shows that the SiNW has a resistivity of 0.021 Ω·cm, and the resistance per SiNW is 130 kΩ. Next, an extra SiO_2 layer of 400 nm is deposited for protection. After via opening and Al metal patterning, the device is released by hydrogen fluoride (HF) vapor, with the HF etching away the BOX layer between U-shape NEMS switch and silicon substrate. Therefore, the gap of the switch is defined by the thickness of the BOX layer.

After the release process, the NEMS switch is checked under the scanning electron microscope (SEM). The SEM photo in Fig. 1(b) shows a clean release process and the residues could be considered as acceptable. The surface of the substrate has not been attacked, and the two Si contact surfaces remain smooth and unaffected by the fabrication processes. The metal line and contact with SiNW are well survived. No stiction or deflection could be found for SiNWs while the paddle, which is made from single crystal Si, remains free-standing above the substrate.

Fig. 2 shows the I-V plots of the fabricated U-shape NEM switch. Since it is operated as a two-terminal switch, the voltage applied is between the U-shape structure and the substrate. The voltage is swept from 0–3 V, with no compliance being set for the current. The measured off current is around 10 pA, which is equivalent to the noise level of the testing setup. The first pull-in happens at 1.81 V, causing the current to increase rapidly to 0.1 μA. Based on the applied voltage step of 10 mV, this abrupt switching slope is less than 4 mV/decade. This represents ideal on/off current characteristic, where the sub-threshold slope is substantially lower the theoretical limit of CMOS devices (60 mV/decade), and it also provides a voltage range in which the off current is always limited to the noise level i.e., negligible. The current continues to increase rapidly to 3 μA, which is quite common in Si-Si contact. The on state current also



Sweep	Pull-in voltage(V)	Current ratio
1	1.81	595
2	1.31	392
3	1.55	1320
4	0.78	22
5	1.21	11603

FIG. 2. (Color online) I-V characteristic of the device shown in Fig. 1(b) for the first five switching cycles. The current ratio indicates the change in current that occurs within 10 mV of the pull-in voltage.

indicates the resistance of the current loop to come mainly from the contact, which should be in the range of few hundreds of kΩ. Hence, taking into consideration of our initial measurement results, our proposed U-shape NEM switch can be considered to be very attractive for low power applications due to its nearly zero leakage current and abrupt switching characteristics. It has a well-defined off-state range and the low pull-in voltage indicates its good compatibility with modern CMOS devices.

The following switching cycles also show a good switching behavior. The ON/OFF state current maintains at the same level for every cycle. The average pull-in voltage is 1.12 V. The pull-in voltage varies in a wide range of about 1 V. A possible reason for such pull-in voltage variation is the charging effect on the native oxide that has grown on the contact surface. During the electrical measurement, charges can be stored on these surfaces and an additional electrostatic force is formed to decrease the initial gap. It also explains the reason why the first pull-in voltage is much larger than all the following sweeps after it. Such kind of phenomenon cannot be avoided after HF vapor releasing for Si-Si contact working in ambient air condition. However, adding process to cover the contact by metal before release would improve the performance of the U-shape NEMS switch largely, as it could avoid the charging issue and provide a much lower contact resistance.

However, we also observed that the nearly zero off-current characteristics of the U-shape NEM switch starts to deteriorate after five switching cycles (Fig. 3). As the current go through the SiNW increase to 3 μA, the nanowire suffers from accumulative Joule heating effect after taking into consideration of its extremely small cross-section area. The oxide insulating layer just behind the SiNW would be physically damaged and eventually become welded in ambient air. The device manages to operate for 12 cycles before no switching behavior is observed. The endurance property would be greatly improved if an insulating layer of high melting point and strong hardness is used instead.

Fig. 4 shows the COMSOL simulation performed to estimate the effect on the variation of SiNW length. The size of the capacitive paddle and the gap are fixed in the simulation. When the length of SiNW equals to zero, which means

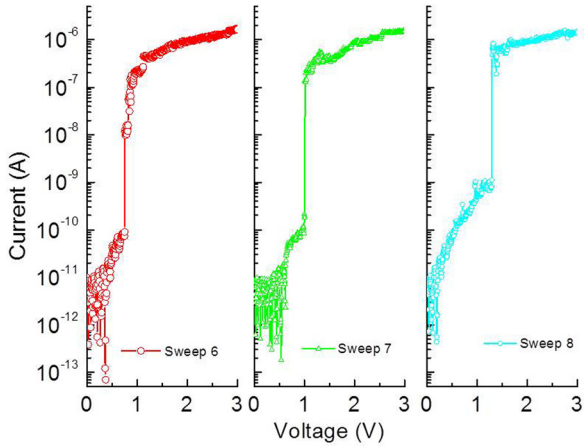
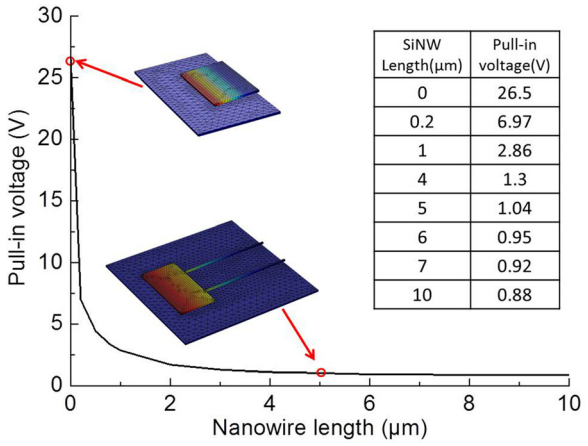


FIG. 3. (Color online) I-V characteristic of the device, with deterioration in off-state current during the 6 to 8 switching cycles.



SiNW Length(μm)	Pull-in voltage(V)
0	26.5
0.2	6.97
1	2.86
4	1.3
5	1.04
6	0.95
7	0.92
10	0.88

FIG. 4. (Color online) Simulated result for the influence on nanowire length versus pull-in voltage, as the length of SiNW varies from 0 μm to 10 μm.

the movable part is only the capacitive paddle and the paddle is fixed at one end becoming a simple fix-free cantilever. The pull-in voltage of such cantilever type of switch increases to as high as 26.5 V. When a very short SiNW with length of 0.2 μm is included in simulation, the pull-in voltage dramatically decreases to 6.97 V. In addition, simulation result has shown that our design has great effectiveness in reducing the pull-in voltage as SiNW length increasing 5 μm. Once the length of SiNW exceed 5 μm, the pull-in voltage become saturated, without significant improvement in the performance in term of pull-in voltage, and the paddle with a softer support structure suggests it would be easier to collapse. Therefore, a better approach to further reduce the pull-in voltage will be to enlarge the capacitive paddle.

In conclusion, our reported a dual SiNWs based U-shape NEMS switch shows excellent result in terms of lowering down the actuation voltage. We take advantage of the high electrostatic force generated from the large capacitive paddle and high flexibility from the single crystal SiNW. The device shows great potential on the voltage compatibility with modern CMOS circuit. Further amendment with better insulting layer and contact material is possible so as to achieve a higher reliability and performance. Furthermore, both CMOS compatibility and ultra-low power consumption provide better integration with different kinds of devices.

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