Seal and encapsulate cavities for complementary metal-oxide-semiconductor microelectromechanical system thermoelectric power generators

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This article presents a method for fabricating thermoelectric power generators (TPGs) using wafer-level vacuum sealing and encapsulation at low temperature with complementary metal-oxide-semiconductor compatible processes and materials. A novel TPG design with thermal legs embedded in top and bottom vacuum cavities is proposed. Simulation results validate that the two cavities can maximize the temperature difference between the hot and cold junctions of thermocouples. Process flows for wafer-level sealing and encapsulating cavities are presented and a thermoelectric power generator is developed based on heavily *p*- and *n*-doped polysilicon. A power generation factor of 0.052 $\mu W\ cm^{-2}\ K^{-2}$ was achieved using this TPG. *© 2011 American Vacuum Society.* [DOI: 10.1116/1.3556954]

I. INTRODUCTION

Thermoelectric power generators (TPGs) transform thermal energy into electrical energy. In the complementary metal-oxide-semiconductor (CMOS) microelectromechanical system (MEMS) TPGs, planar thermopiles are arranged on the top of a substrate because thermoelectric material thicknesses are limited in the ranges that can be achieved by thin-film technology. Cavities are created to guide heat flux along the longitudinal direction of thermal legs.[1–4] To reduce heat loss by convection, the cavities are required to be sealed in high vacuum. Recently, researchers have proposed methods for low-temperature wafer-level sealing to create sealed vacuum cavities. For example, Stark and Najafi[5] demonstrated a packaging technology that employs an electroplated nickel film to vacuum seal a MEMS structure at the wafer level. The package was fabricated at low temperature ($<250\ ^\circ C$) by electroplating a 40-μm-thick nickel film over an 8 μm sacrificial photoresist that was removed prior to package sealing. Monajemi *et al.*[6] presented a low-temperature (260 °C) packaging technique that utilized thermal decomposition of a sacrificial polymer through a gas-permeable polymer overcoat to form a released thin-film organic membrane with scalable height on top of the active part of the MEMS. However, these technologies are so-called post-CMOS processes and materials are not available in the standard CMOS manufacturing line. In the conventional CMOS-compatible approaches, the cavity is sealed by low-pressure chemical vapor deposition (LPCVD) films (polysilicon and nitride) at temperatures above 570 °C.[7] However, if the sealed device has aluminum interconnection, the maximum temperature cannot be higher than 400 °C. To limit the processing temperature under 400 °C, most researchers seal cavities with plasma-enhanced chemical vapor deposition (PECVD) films. For example, Buchwalter *et al.* developed Bi-CMOS-compatible process for the fabrication of MEMS resonators and filters, wherein the cavity was sealed with PECVD film at 400 °C, making the devices possible to be integrated directly on chip without affecting the existing analog circuitry.[8]

In this paper, we present methods for wafer-level vacuum sealing and encapsulation with CMOS-compatible process and materials for fabrication of TPGs. First, we conduct simulations to validate the performance improvement contributed by top and bottom vacuum cavities. Following, a CMOS-MEMS TPG is fabricated by embedding thermocouples between two microscale vacuum cavities, which are sealed at 400 °C and at a vacuum level of 2.4 Torr. Finally, the output power is measured by applying temperature difference across the fabricated TPG.

II. DESIGN

The proposed TPG is composed of polysilicon thermopiles embedded between top and bottom cavities,[9] as shown in Fig. 1. The bottom cavities guide the heat flux through thermal legs, while the top cavities protect hot junctions from being cooled by air convection. In contrast, the area of

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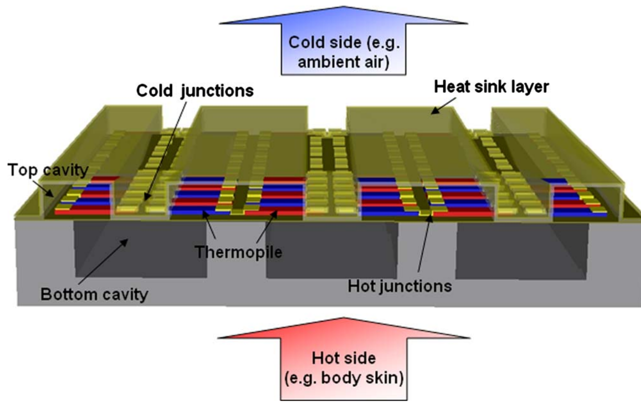

FIG. 1. (Color online) Schematic view of the proposed TPG with configuration of top and bottom cavities.

cold junctions is exposed to ambient air. Both the bottom and top cavities are sealed with high vacuum level to minimize heat loss due to heat conduction and convection through air. With such a design, the planar thermopiles work like a vertical configuration.

The output power P_o is given by

$$P_o = \frac{m^2\alpha^2}{4R_G}\Delta T_G^2 \tag{1}$$

and is achieved under matched load resistance; i.e., the internal resistance of the generator R_G is equal to the load resistance connected to the generator. In Eq. (1), m is the number of thermocouples, α is the relative Seebeck coefficient, and ΔT_G is the temperature difference between the hot and cold junctions. Three-dimensional models were built with the software ANSYS for thermal finite-element analysis. In the finite-element simulations, a fixed temperature difference of 5 K between the top and bottom of the device is assumed as boundary conditions for thermal analysis. Simulations are conducted for four possible configurations: the first one, which is proposed in this paper, has top and bottom vacuum cavities [Fig. 2(a)] and ΔT_G=3.75 K; the second one has top and bottom cavities full of air [Fig. 2(b)] and ΔT_G=2.77 K; the third one has only a bottom vacuum cavity [Fig. 2(c)] and ΔT_G=1.72 K; and the last one has only top vacuum cavity [Fig. 2(d)] and ΔT_G=0.95 K. Since output power is a second order function of the temperature difference, the output power is greatly improved by the formation of the vacuum cavities.

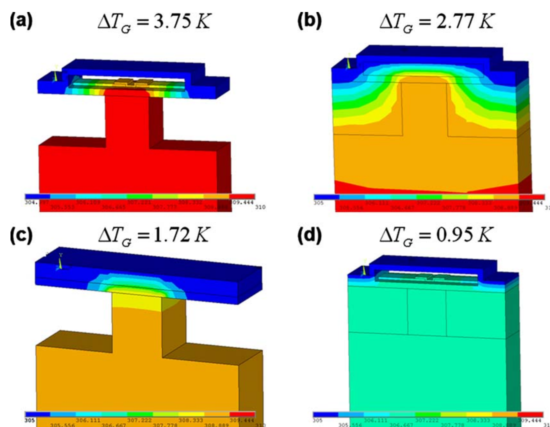

FIG. 2. (Color online) Simulated temperature distribution for four designs: (a) with top and bottom vacuum cavities, ΔT_G=3.75 K; (b) with top and bottom air cavities, ΔT_G=2.77 K; (c) with only bottom vacuum cavity, ΔT_G=1.70 K; and (d) with only bottom vacuum cavity, ΔT_G=0.95 K.

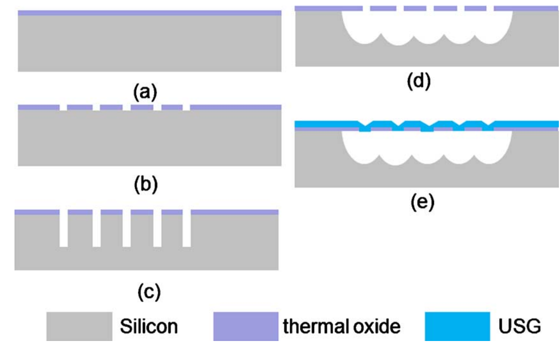

FIG. 3. (Color online) Verification process flow for sealing a 15-μm-deep bottom cavity with PECVD USG.

III. PROCESSES OF WAFER-LEVEL SEALING AND ENCAPSULATION

The fabrication challenge in making the proposed thermoelectric power generator is creating the bottom and top cavities. In this section, the methods for sealing the bottom vacuum cavity and encapsulating the top vacuum cavity are introduced. To create the bottom vacuum cavity, a 0.2-μm-thick SiO_2 hard mask is grown by thermal oxidation [Fig. 3(a)] and patterned with 1-μm-wide openings [Fig. 3(b)]. 15-μm-deep trenches are etched into the silicon substrate using deep reactive ion etching (DRIE) with SF_6 and C_4F_8 gases [Figs. 3(c) and 4(a)]. Following, the wafer is isotropically etched using SF_6 plasma to remove the silicon

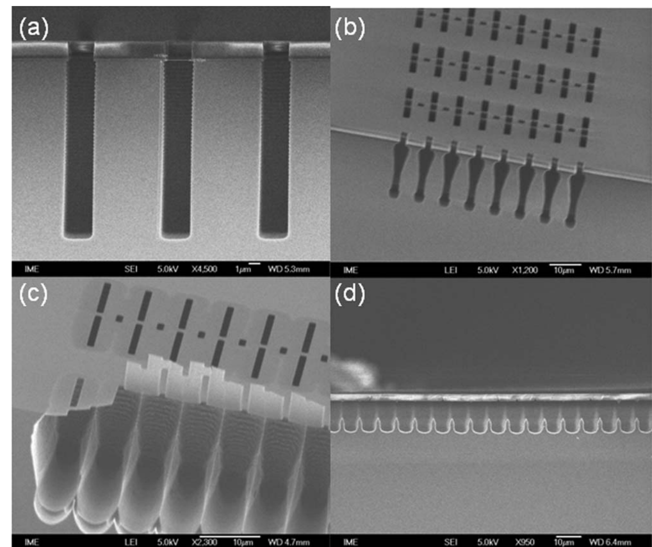

FIG. 4. SEM images at different steps of the verification process for sealing the bottom vacuum cavity.

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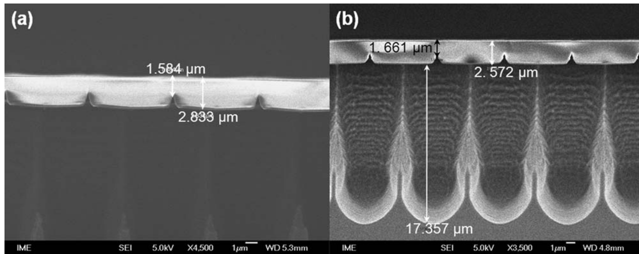

FIG. 5. Comparison of cavity sealing methods with PECVD (a) USG and (b) reflowed PSG.

between the trenches to form the bottom cavities [Figs. 3(d), 4(b), and 4(c)]. Finally, the bottom cavities are sealed using a 2.5-μm-thick low stress undoped silicate glass (USG) film deposited by PECVD at 400 °C [Figs. 3(e) and 4(d)]. The vacuum level in the cavities is the process pressure in the PECVD reaction chamber, i.e., 2.4 Torr.

PECVD phosphorous silicate glass (PSG) is usually used to seal cavities due to its reflow capability at temperature around 1000 °C. The sealed surface with reflowed PSG is smoother than that achieved with USG, as shown in Figs. 5(a) and 5(b). However, USG is chosen for the fabrication of device because metal interconnections cannot stand the high temperature of PSG reflow. In addition, the residual stress of USG is lower than the one of PSG. Stress is a critical problem in fabrication of CMOS-MEMS devices. High stress will cause wafer warping so that further processes cannot proceed.

To create the top vacuum cavity, a 4-μm-thick low stress USG is deposited by PECVD and patterned [Fig. 6(a)]. In the following, another 0.5-μm-thick USG layer is deposited as stepper and patterned [Fig. 6(b)]. The USG layers are covered by 0.7 μm PECVD Si_3N_4 and 0.2 μm amorphous silicon films [Figs. 6(c) and 7(a)]. Small 1×3 μm^2 etching holes are etched through the nitride and the amorphous silicon films [Fig. 6(d)]. Thereafter, the wafer is dipped in the buffered oxide etchant (BOE) for about 20 min to remove the sacrificial USG layer via the etching holes [Figs. 6(e) and 7(b)]. Finally, the holes are sealed by a 2.5-μm-thick PECVD low stress USG [Figs. 6(f) and 7(c)]. Cross-sectional view shows that the cavity is completely sealed [Fig. 7(d)].

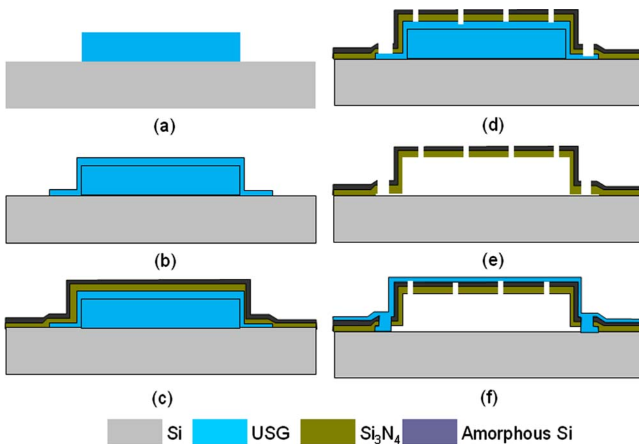

FIG. 6. (Color online) Verification process flow for encapsulating a 4.5-μm-high top cavity with PECVD USG.

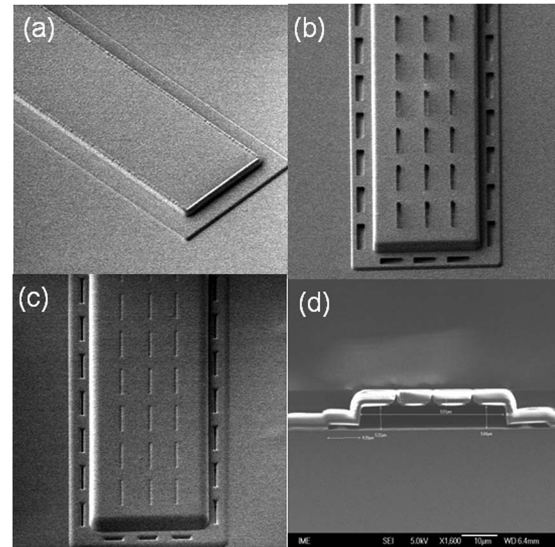

FIG. 7. SEM images at different steps of the verification process flow for encapsulating top vacuum cavity.

LPCVD nitride is usually used to form the shell of the cavity due to its low etching rate in BOE. However, wafer with metal interconnection cannot be processed in LPCVD. If only PECVD nitride is used as the shell material, the shell cannot survive in BOE. Figure 8 shows that 0.7 μm PECVD nitride cannot resist BOE etching for 5 min. Therefore, a 0.2-μm-thin amorphous silicon film, which has very low etching rate in BOE, is used on the PECVD nitride to protect the shell structure. The shell made of PECVD nitride and amorphous silicon can withstand BOE etching for more than 30 min.

IV. FABRICATION OF THERMOELECTRIC POWER GENERATOR

Using the wafer-level sealing and encapsulation methods described and demonstrated above, a CMOS-MEMS TPG is

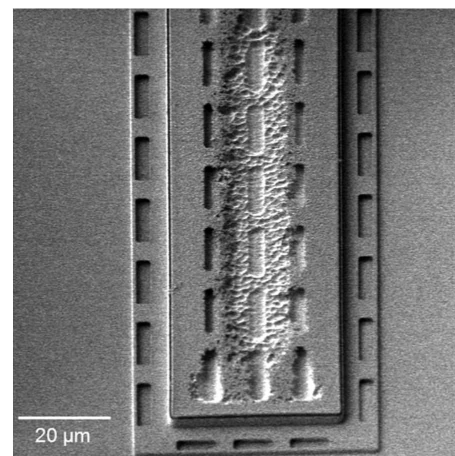

FIG. 8. Shell made with PECVD nitride fails to survive in BOE.

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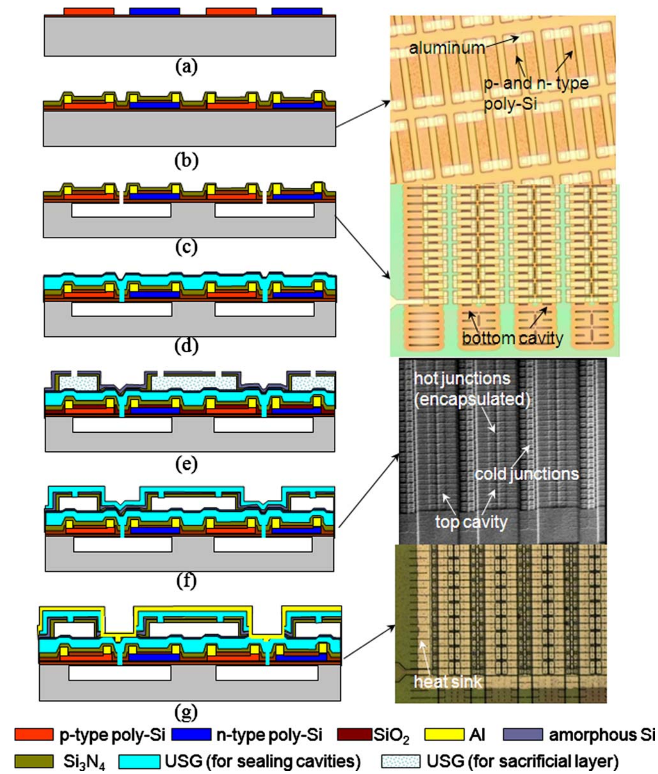

FIG. 9. (Color online) Whole fabrication process flow of the TPG and images at the different steps.

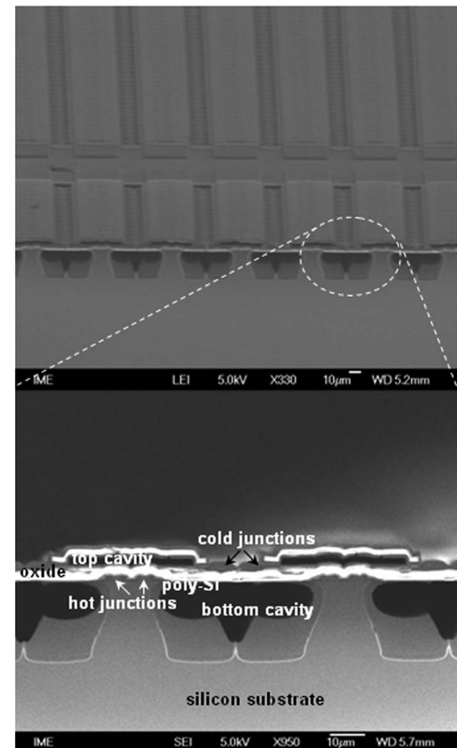

FIG. 10. Cross-section view of the fabricated TPG with 2-μm-high top cavity and 30-μm-deep bottom cavity.

fabricated. The main process steps and images are illustrated in Fig. 9. The 0.7-μm-thick poly-Si is deposited at 580 °C in furnace by LPCVD as the thermoelectric layer. In the following, the poly-Si layer is dry etched to form thermoelectric leg patterns with 5 μm in width and 16 μm in length [Fig. 9(a)]. Afterward, the poly-Si layer is partially implanted with phosphorous ions at 180 keV energy to generate the *n*-type thermoelectric legs. Poly-Si is subsequently implanted with boron ions using 80 keV in the other half to form the *p*-type thermoelectric legs. The doping dose of 10^{16} cm^{-2} is used in both steps. The doped poly-Si is annealed in a furnace at 1000 °C for 30 min. After SiO_2 insulating layer deposition and contact via opening, aluminum layer is deposited and etched to form electrical interconnects between the *p*-type and *n*-type thermoelectric legs in series, as shown in Fig. 9(b). The bottom cavity and top cavity are created with the prementioned processes of wafer-level sealing and encapsulation: first perforating the holes, DRIE, and isotropic etching silicon [Fig. 9(c)], sealing bottom cavities [Fig. 9(d)], patterning USG sacrificial layer, opening etching holes [Fig. 9(e)], and finally removing the USG sacrificial layer and sealing the top cavities [Fig. 9(f)]. In the last step, 0.7-μm-thick aluminum is deposited to cover the whole device area as the heat sink layer [Fig. 9(g)]. The layer infor-

TABLE I. Layer information of the fabricated TPG.

No.	Material	Process	Description	Thickness (μm)
1	Oxide	Thermal oxidation	Insulating layer	0.1
2	Poly-Si	LPCVD	Thermal leg	0.7
3	Aluminum	Sputtering	Interconnection	0.75
4	Oxide	PECVD	Insulating layer	0.2
5	Nitride	PECVD	Passivation	0.3
6	Low stress USG	PECVD	Sealing bottom cavities	2.5
7	Amorphous silicon	PECVD	Protection layer in BOE	0.15
8	Low stress USG	PECVD	Sacrificial layer	2.5
9	Nitride	PECVD	Shell of top cavities	0.7
10	Amorphous silicon	PECVD	Shell of top cavities	0.2
11	Low stress USG	PECVD	Sealing bottom cavities	2.5
12	Aluminum	Sputtering	Heat sink	0.75

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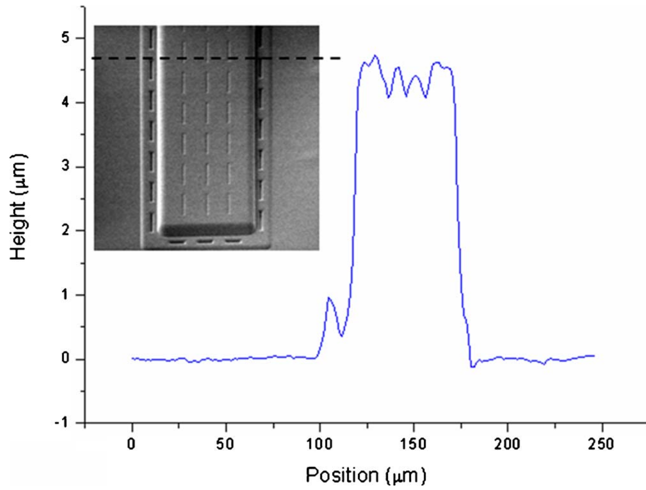

FIG. 11. (Color online) Surface profile of the sealed cavity shows that the membrane is strong enough to withstand the vacuum force.

mation including the deposition method and the thicknesses are summarized in Table I. The cross section of the fabricated device in Fig. 10 shows that the thermal legs are embedded into the top cavities and the bottom cavities. The sealed bottom cavity is about 30 μm deep and 42 μm wide, while the encapsulated top cavity is 2 μm high and 35 μm wide. The lengths of both bottom and top cavities are about 670 μm. Step height is limited by the inability of contact photolithography to resolve fine patterns on a high topography. In the fabrication of the complete device, more layers are deposited and patterned than those in the process that was used to develop and verify the sealing method. All these patterned layers add to the step height. As a result, the maximum cavity height achieved in the final device is 2 μm, which is lower than 4.5 μm, the height achieved in the verification process.

V. TESTING

The membrane that caps the cavity deforms due to the different pressures between the two sides of the membrane. If this membrane is too flexible, the vacuum force will push it into contact with the generator thermopile, leading to malfunction. In the fabricated device, the USG cap membrane is 2.5 μm thick, 35 μm wide, and 670 μm long. To inspect the deformation, surface profile of the sealed top cavity is measured by an optical profiler (Wyko NT3300), as shown in Fig. 11. The maximum bending is at the center of the cap and

TABLE II. Characterization of thermoelectric properties for polysilicon at $T=300$ K.

Material	Electrical resistivity (Ω μm)	Seebeck coefficient (μV/K)	Thermal conductivity (W m^{-1} K^{-1})	Figure of merit
p-type polysilicon	13.7	130	28.4	0.012
n-type polysilicon	8.9	−110	29.7	0.014

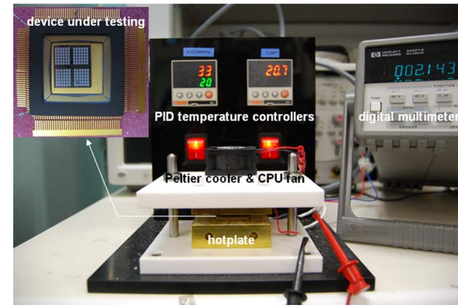

FIG. 12. (Color online) Testing setup for temperature control and voltage measurement and the 1×1 cm^2 device with wire bonding for testing.

is only 0.2 μm, much smaller than the 2 μm cavity height. Thus, the membrane cap in the device is strong enough to withstand the vacuum force.

Polysilicon was characterized to evaluate its thermoelectric properties at 300 K. Electrical resistivity, ρ, was measured using the van der Pauw configuration, the Seebeck coefficient, α, was extracted from a planar test structure, and thermal conductivity, λ, was determined using a cantilever test structure.[9] These results are shown in Table II. The thermoelectric figures of merit $ZT=(\alpha^2/\rho\lambda)T$ for *p*-type and *n*-type polysilicon were determined to be 0.012 and 0.014, respectively.

The device chips under testing were diced into 1×1 cm^2 pieces. Each chip included 125 144 thermocouples with total internal resistance of 52.8 MΩ. The measurement setup is depicted in Fig. 12. The device under testing was placed between a hotplate and a brass heat sink, which was cooled by a Peltier cooler. A CPU fan is mounted to disperse the heat from the cooler to ambient air. Two PT100 temperature sensors were integrated into the hotplate and heat spreader for sensing temperature. The temperature difference and range can be adjusted via two proportional-integral-derivative controllers driving the hotplate and the Peltier

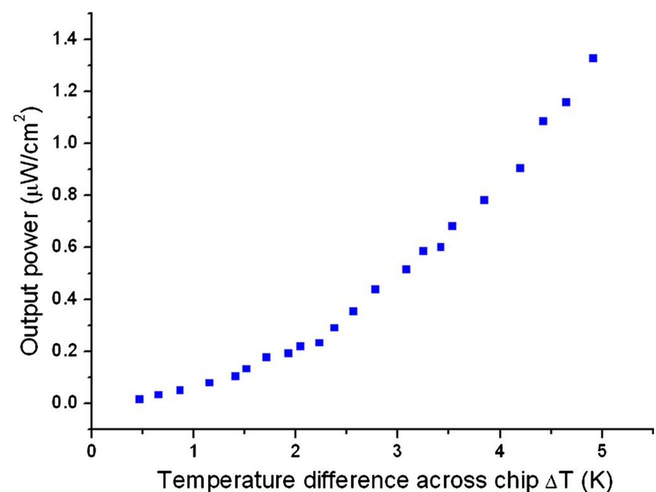

FIG. 13. (Color online) Output power vs temperature difference under a matched electrical resistance load.

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TABLE III. Comparison with CMOS-compatible TPGs in the literature.

	Thermoelectric materials	Power generation factor (μW cm^{-2} K^{-2})
Ref. 1	Poly-Si	0.042 6
	Poly-SiGe	0.035 2
Ref. 2	Al/poly-Si	0.003 63
Ref. 3	Poly-Si	0.041 7
Ref. 4	Poly-SiGe	0.002 6
This work	Poly-Si	0.052

cooler separately. A Hewlett Packard 34401A digital multimeter is used to record the internal resistance and the output voltage.

A graph of the output power per device area versus temperature difference and the TPG prototype are displayed in Fig. 13. When 5 K difference is maintained across two sides of a 1 cm^2 device, the output power is 1.3 μW under a matched electrical resistance load, 1.3 times higher than the power from the polysilicon TPG reported in Ref. 1. The calculated power generation factor is 0.052 μW cm^{-2} K^{-2}. Table III shows the comparison with CMOS-compatible thermoelectric power generators in the literature. In the *I-V* curve shown in Fig. 14, as expected for a thermoelectric generator, the voltage decreases linearly, while the output power rises to a maximum (about 1.3 μW) before decreasing. At zero load resistance the current produced is 0.31 μA.

VI. CONCLUSION

Methods for wafer-level vacuum sealing and encapsulation with CMOS-compatible process and materials have been presented. The cavities are sealed at 400 °C and the vacuum level is 2.4 Torr. Using these methods, a novel thermoelectric power generator is developed. The thermal legs are embedded between the top and bottom cavities. With such a design, the heat flux along thermal legs is optimized and the temperature difference between the two junctions of thermal couples is maximized. The whole fabrication process is CMOS compatible. The fabricated power generator has a power generation factor of 0.052 μW cm^{-2} K^{-2} and may be used as a novel on-chip power source for self-powered CMOS and MEMS devices that have low power consumption requirements.

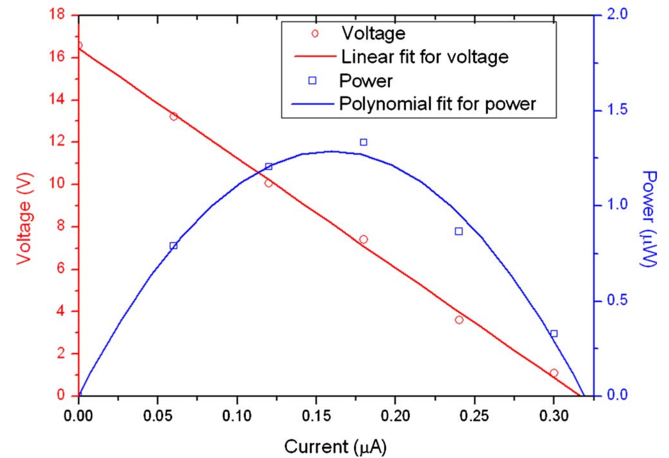

FIG. 14. (Color online) Output power and voltage vs current at a temperature difference of $\Delta T=5$ K.

ACKNOWLEDGMENT

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