Microsyst Technol (2011) 17:77–83
DOI 10.1007/s00542-010-1183-9

TECHNICAL PAPER

Microstructures for characterization of seebeck coefficient of doped polysilicon films

Jin Xie · Chengkuo Lee · Ming-Fang Wang · Julius Minglin Tsai

Received: 1 July 2010 / Accepted: 6 December 2010 / Published online: 17 December 2010

Abstract CMOS based thermoelectric micro-transducers have been demonstrated for various applications. To achieve better design and optimization of such micro-transducers, the Seebeck coefficient of doped polysilicon thin film needs to be measured accurately with respect to optimization effort in process and structure design of micro-transducers. A novel circular test structure is firstly presented to get accurate value of Seebeck coefficient in this paper, while the known planar and cantilever test structures are fabricated together and characterized separately to validate the measured Seebeck coefficient of samples with the same process conditions for comparison. Seebeck coefficient measured by the circular structure shows good agreement with the result measured by cantilever structure, while there is an error of about 14% for the result given by planar structure. The circular test structure is a good at accurate testing of the average absolute values of Seebeck coefficient of p-type and n-type. Strength and drawback for the three structures are summarized.

1 Introduction

The Seebeck effect is known as the conversion of temperature differences directly into electricity. By using the thermoelectric (Seebeck) effect, diversified micro-transducers, such as IR detector (Socher et al. 2000; Du and Lee 2000; Hirota et al. 2007), thermoelectric power generator (Yang et al. 2009, 2010; Wang et al. 2009a; Xie et al. 2010) and Peltier cooler (Baltes et al. 1998; Huang et al. 2008) have been reported. Heavily doped polysilicon have been widely used as thermoelectric material due to that it's Complementary-Metal–Oxide–Semiconductor (CMOS) material and it gives high Seebeck coefficient. To improve the performance of the thermoelectric devices, thermoelectric properties of doped polysilicon need to be characterized and optimized. By using commercial CMOS IC processes, Arx et al. (1997) reported measured Seebeck coefficient of polysilicon over a wide temperature range from 120 to 400 K based on planar and cantilever test structures. Mancarella et al. (2006) proposed a method aimed at executing accurate Seebeck coefficient measurements at the wafer level on the cantilever test structures without resorting to vacuum environment. Boutchich et al. (2002) characterized Seebeck coefficient of boron and phosphorous heavily doped low pressure chemical vapour deposition (LPCVD) polysilicon films with different doses in the temperature range of 293–373 K. Strasser et al. (2004) demonstrated micromachined thermoelectric power generator using thermocouples made of polysilicon and characterized the Seebeck coefficient at different doping concentrations in 2004. Xie et al. (2009) characterized Seebeck coefficient of boron and phosphorus doped LPCVD polysilicon films with doping doses from 4×10^{15} to 10×10^{15} at/cm^2 for the application of thermoelectric power generators. Additionally, PolySiGe, as another CMOS compatible material, has also been characterized for Seebeck coefficient (Wijngaards and Wolffenbuttel 2002; Wang et al. 2009b; Arx et al. 2000).

Generally the Seebeck coefficient measurement is based on the following method. Firstly a sample with integrated

J. Xie (✉) · C. Lee · M.-F. Wang · J. M. Tsai
Institute of Microelectronics, A*STAR (Agency for Science, Technology and Research), 11 Science Park Road, Singapore Science Park II, 117685 Singapore, Singapore
e-mail: xiej@ime.a-star.edu.sg

C. Lee
Department of Electrical and Computer Engineering, National University of Singapore, 4 Engineering Drive 3, 117576 Singapore, Singapore

polysilicon test pattern is micromachined, and then metallization process is finished to give metal contacts at the two ends of polysilicon layer pattern. A polysilicon heater is placed closely to one end and it can enable the temperature of this end of polysilicon test pattern to be increased by ΔT above the temperature of the other end, i.e., cold end, when a current is passing through the polysilicon heater. As a consequence of that, a thermoelectric voltage U arises across the polysilicon test pattern. By measuring the temperature difference with the reference temperature given by a thermistor, the Seebeck coefficient can be calculated as

$$\alpha|_{\frac{T_h+T_c}{2}} = \frac{U}{T_h - T_c} = \frac{U}{\Delta T} \quad (1)$$

In previous reports (Baltes et al. 1998; Arx et al. 1997; Mancarella et al. 2006; Xie et al. 2009), planar and cantilever test structures have been investigated for measuring Seebeck coefficient. A new circular test structure is firstly presented in this paper, while planar and cantilever test structures were discussed later to validate the measured data of circular test structure.

2 Circular test structure

In order to get rid of the discrepancy in the measured data due to the wafer process, these three test structures are fabricated in one 8″ wafer in the adjacent area. Thus we arranged the layout of three test structures in the mask as shown in Fig. 1. The microfabricated circular test structure containing multiple thermal legs is shown in Fig. 2. There are total five pairs of n-type and p-type polysilicon thermal legs which are electrically connected in series in a radial formation. A circular cavity is created by silicon etching, so that one end of the thermal leg is suspended on the center membrane (hot end) and the other end is on the silicon substrate (cold end). Two circular resistors made of polysilicon are integrated into the center suspended membrane. The inner resistor at the center is used as a heater, and the outside resistor is used as temperature monitoring sensor. When the heating resistor is applied with electrical current (via pads 5 and 6), the temperature of the hot junctions is increased and measured through the temperature monitor resistor (via pads 3 and 4). Because the cold junctions are located above the thermally highly conductive silicon substrate, its temperature is assumed as room temperature. The thermovoltage between the two ends of thermopile is measured simultaneously (via pads 1 and 2). Finally, Seebeck coefficient can be calculated from the ratio of thermovoltage to temperature difference of the two junctions. It is noted that the calculated Seebeck coefficient is an average absolute values of n- and p-type polysilicon. For the applications of thermoelectric power generator and Peltier cooler, these devices work based on thermal couple, instead of single type of thermal legs. Therefore, average absolute Seebeck coefficient of p- and n-type thermal legs is sufficient to describe material property for the above applications.

To prepare polysilicon samples for testing, 700 nm thick polysilicon layers are grown at 580°C in furnace by LPCVD. The poly-Si layer is partially phosphorous-implanted with an energy of 180 keV to generate the n-type thermoelectric legs and is subsequently boron-implanted using 80 keV in the other half region to form the p-type thermoelectric legs. The doping dose of 10^{16} cm^{-2} is used in both steps. Afterwards, the doped polysilicon layers are annealed in furnace at 1,000°C for 30 min to active dopants and obtain a uniform doping profile through the whole thickness and repair the defects in the crystalline structure. After SiO_2 insulating layer depositing and contact via opening, aluminum layer is deposited and etched to

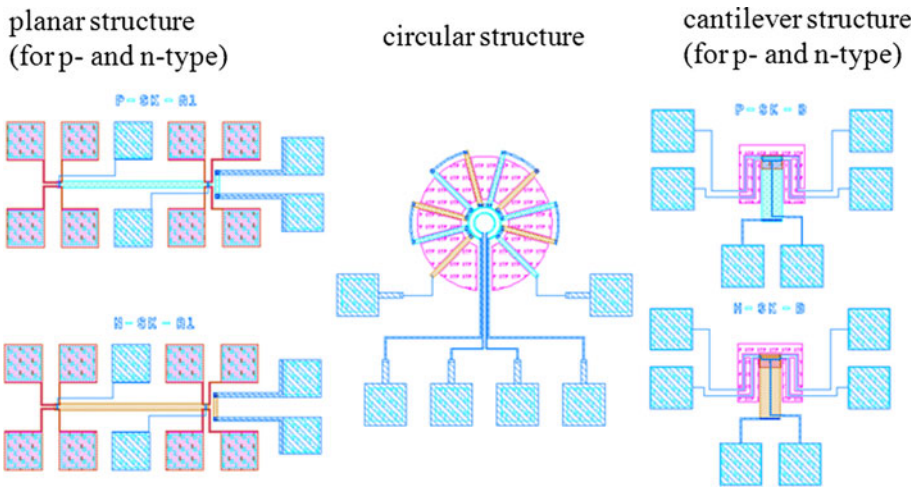

Fig. 1 Layout of the test structures

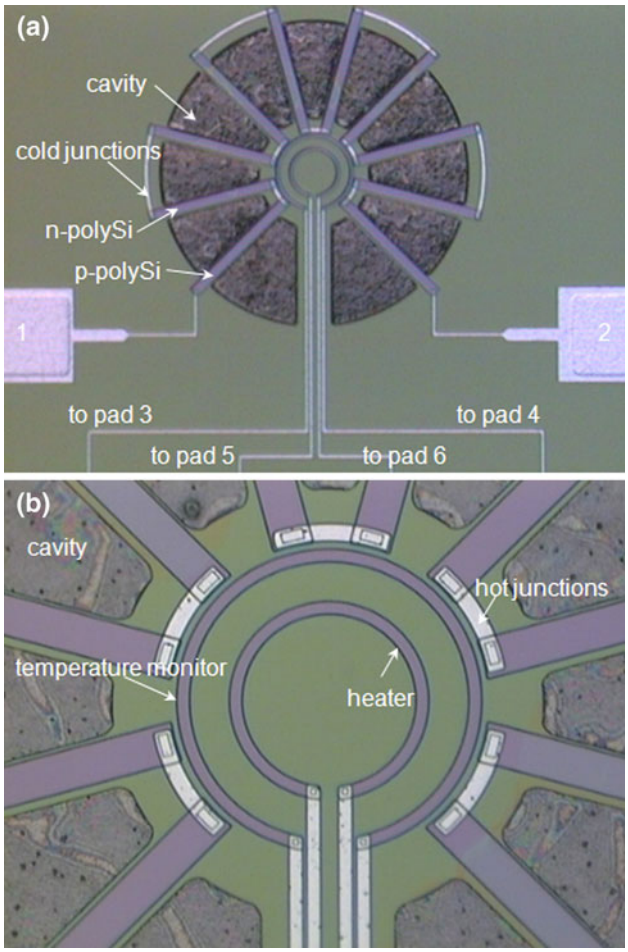

Fig. 2 **a** Circular test structure to determine Seebeck coefficient and (**b**) a close-up view of the center membrane

form electrical interconnects between the p-type and n-type thermoelectric legs in series. Finally, the cavity is created by isotropic silicon etching with XeF_2 gas.

A finite-element simulation of the test structure temperature distribution is done in CoventorWare, as shown in Fig. 3. The heater current applied was 1.5 mA. Peltier effect and Joule heating were included in the simulation model. The bottom side of the chip is set as the room temperature, i.e., 300 K. As it is observed, the maximum temperature increase located at the hot junctions and cold junctions is roughly 13 K. From the results, the temperature turns out to be quite uniform on the temperature monitoring sensor and on the hot junctions. The temperature at cold junctions is 300.3 K. The assumption that temperature at cold junctions equals to the room temperature is quite reasonable.

The testing was done at wafer-level on the probe station. We determined ΔT using the temperature-dependent resistance $R(T)$ of the temperature monitoring sensors, via their

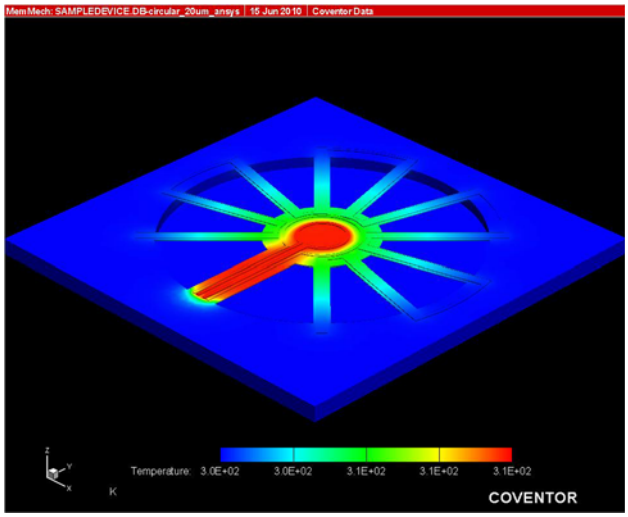

Fig. 3 Finite-element simulation of the circular test structure

temperature coefficient of resistance (TCR)—$\beta(T)$ which is defined as

$$\beta(T) = R(T)^{-1}\frac{d}{dT}R(T) \tag{2}$$

For this purpose, $R(T)$ curves were measured independently for each temperature monitoring sensor of each test structure to take into account possible variations in material properties. Resistance $R(T_i)$ were measured at each temperature T_i $(i = 1, 2,\ldots)$, under stabilized temperature conditions. From the resistance data, values of $\beta(T_i)$, $(i = 2, 3,\ldots)$, were calculated for each temperature monitoring sensor of each test structure using finite difference, i.e.,

$$\beta(T_i) = R(T_i)^{-1}\frac{R(T_{i+1}) - R(T_{i-1})}{T_{i+1} - T_{i-1}} \tag{3}$$

For the thermovoltage measurements, a heating current I_h was passed through the heating resistor. The resulting resistance change ΔR of the temperature monitors was measured simultaneously. The temperature increases ΔT were obtained using,

$$\Delta T = \frac{1}{\beta}\frac{\Delta R}{R} \tag{4}$$

meanwhile, we recorded the output thermovoltage U during the ΔR measurement.

The temperature-dependent resistance of the temperature monitoring sensor and its TCR are shown in Fig. 4. From the resistance and thickness of the polysilicon temperature monitor, we deduced a resistivity of the polysilicon of 11.3 μΩm at 300 K. Its temperature coefficient of resistance is 0.89×10^{-3} K^{-1} at 300 K. Figure 5 shows the experimental data of the thermovoltage and temperature increases at the hot junctions as a function of the

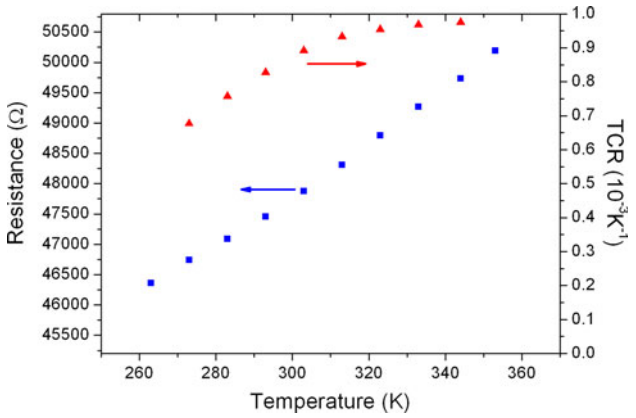

Fig. 4 Temperature-dependent resistance and TCR of the polysilicon temperature monitoring sensor

heating current. When the heating current is 1.5 mA, the temperature difference between hot and cold junctions is 12.2 K, which is slightly lower than the simulation result of 13 K. One reason is the uncertainty of the thermal properties fed into the simulation, and the other reason is that the testing experiment is not conducted in vacuum environment. The measured average absolute Seebeck coefficient at room temperature for a thermocouple made of the doped n- and p-type polysilicon is measured as about 140 μV/K, as shown in Fig. 6.

3 Discussion and comparison of planar and cantilever test structures versus circular test structure

The planar test structure is shown in Fig. 7. The polysilicon stripe test structure being characterized has a length of 670 μm and a width of 30 μm. It is contacted to aluminum at its two ends (pads 5 and 6). An 110 × 20 μm polysilicon heater (pads 11 and 12) is placed 20 μm away from contact of hot junction. Two 5-μm-wide temperature monitors made of aluminum are placed over these two contacts. The temperature monitors are integrated in a four-point measurement configuration (pads 1, 2, 3, 4 and pads 7, 8, 9, 10) enabling accurate measurements of small resistance changes and, thus, small temperature variations. When current is applied to the heating resistor, the temperature of the hot and cold contacts of the polysilicon sample were increased from T_0 to T_h and T_c, respectively. The testing procedure is very similar to the one for circular structure, except that the temperature at cold contact is also needed to measure using a temperature monitoring sensor. However, for this structure, if there is no custom-made probe card, it is difficult to do testing at wafer-level because there is no enough space to allow probing needles of twelve probes on the probe station. Therefore the testing is done after dicing and wire bonding steps. For the p-type polysilicon, the measured

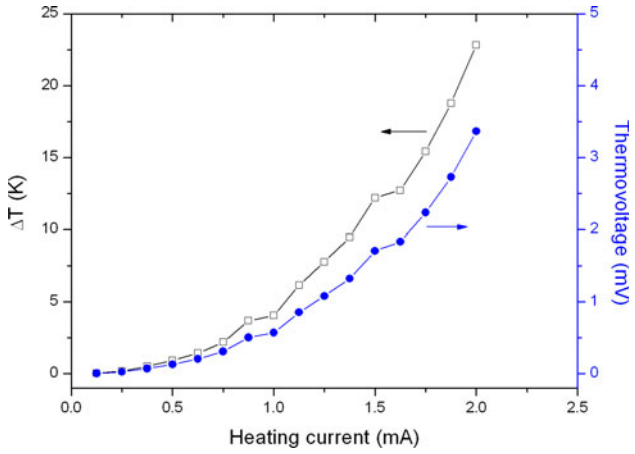

Fig. 5 Temperature difference and thermovoltage versus heating current measured in circular test structure

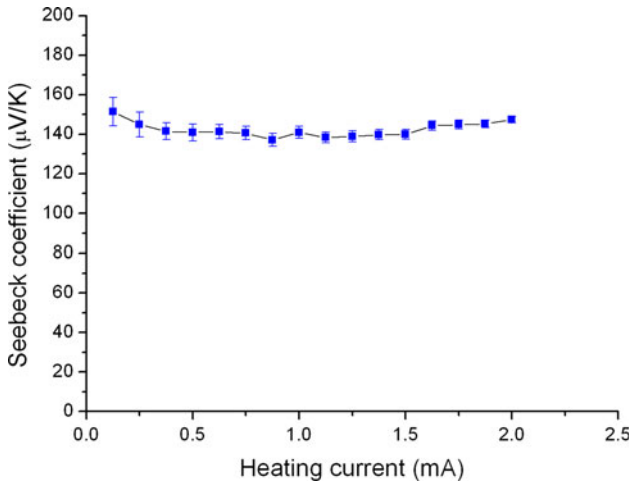

Fig. 6 Average absolute Seebeck coefficient measured in circular test structure

thermovoltage and temperature at hot and cold contacts are shown in Fig. 8. From the calculation of Seebeck coefficients of both p-type and n-type, it is found that for p-type, the Seebeck coefficient is about 130 μV/K, while for n-type, the value is −110 μV/K (Fig. 9 shows the absolute value).

The third test structure for measuring Seebeck coefficient is a cantilever, as shown in Fig. 10. A 100 μm wide and 270 μm long cantilever beam with four narrow arms suspends over a cavity. Two contacts made of aluminum (pads 5 and 6) are used to measure the thermally generated voltage from the polysilicon sample. The hot contact is placed 23 μm away from the tip end of the cantilever, and the cold contact is on the substrate. Two resistors made of polysilicon are integrated into the tip of the cantilever. The resistor (pads 1 and 2) close to the end of the beam is used as a heater, which has length of 92 μm, width of 6 μm and resistance of 2,635 Ω at $T = 300$ K. The other resistor

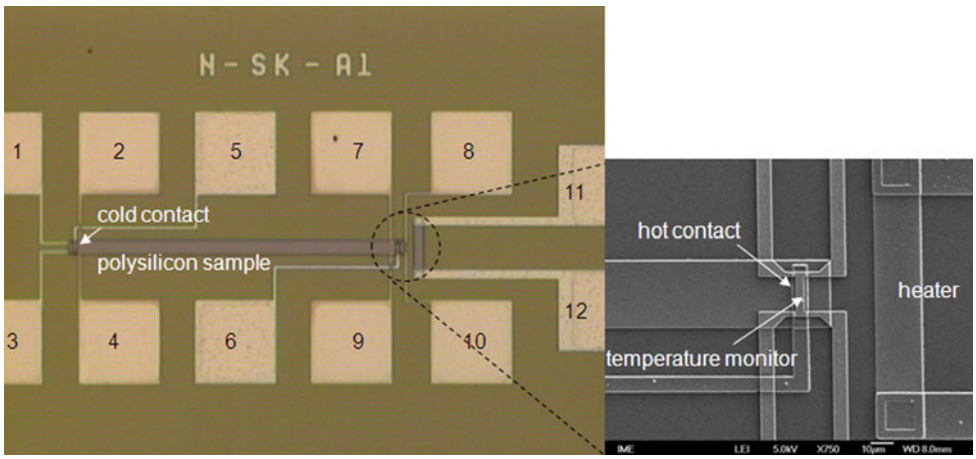

Fig. 7 Planar test structure to determine the Seebeck coefficient

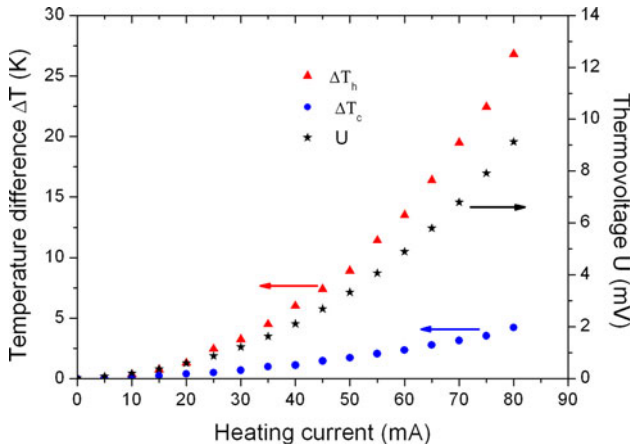

Fig. 8 Temperature difference and thermovoltage measured in planar structure

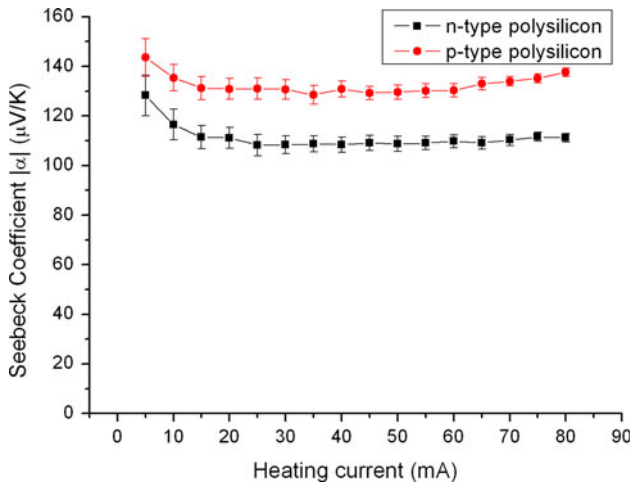

Fig. 9 Seebeck coefficient measured in planar test structure

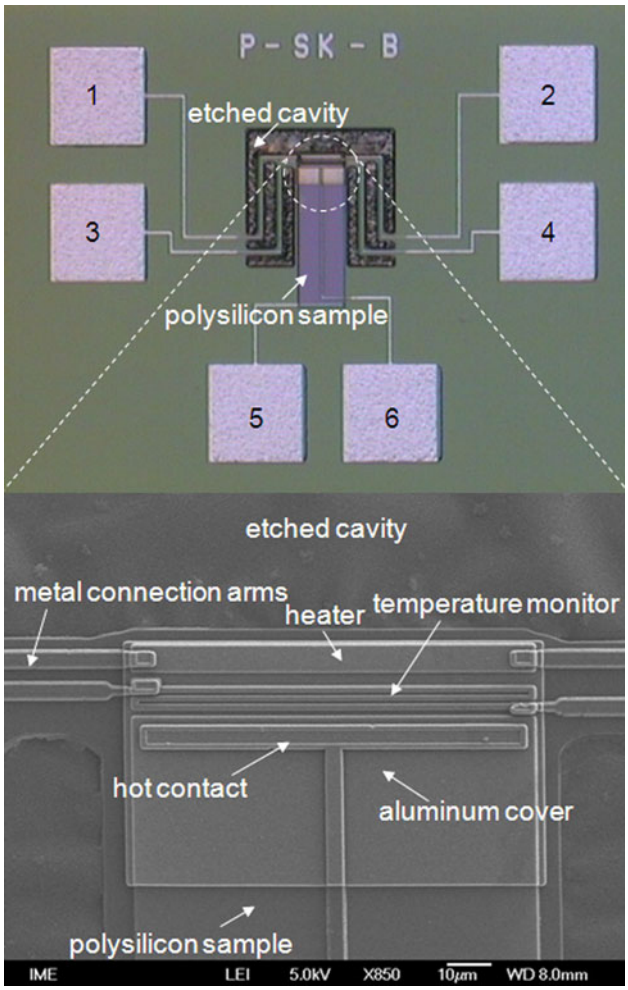

Fig. 10 Cantilever test structure and a close-up view at the tip

(pads 3 and 4) is used as temperature monitoring sensor, with total length of 280 μm and width of 1 μm. The temperature distribution over the top of the two resistors is homogenized with an integrated rectangular cover made of aluminum. This approach minimizes the temperature difference between the hot contact and temperature monitoring sensor. The cantilever structure can also be used to measure thermal conductivity (Xie et al. 2009; Arx et al. 2000). The testing procedure for measuring Seebeck

Table 1 Comparison of the three test structures of measuring Seebeck coefficient

	Fabrication	Power consumption	Thermovoltage	Measurement	Characterization type
Circular	Micromachining	Medium	High	Wafer level	Average absolute values of n-and p-
Planar	Standard thin film processing and structuring	High	Low	Diced chip	n- or p-
Cantilever	Micromachining	Low	Low	Wafer level	n- or p-

coefficient is totally the same as the one for circular structure. The measured Seebeck coefficient is about 155 μV/K for p-type, and about −137 μV/K for n-type.

From circular test structure, we obtained an average absolute Seebeck coefficient (140 μV/K) which is quite close to the result measured from the cantilever structure (146 μV/K). But such a value is a little higher than the value from planar structure (120 μV/K). One reason is that the temperature monitoring sensor is metal with lower resistivity and TCR in the planar test structure. Although four-point method is used to measure the resistance, certain errors still exist. Another reason is that the testing of planar structure was done after device dicing and wire-bonding, while the testing of circular and cantilever structures was done in wafer-level on probe station. The extra resistance brought by wire-bonding will affect the resistance measurement. The planar structure is fabricated only by thin film processing and structuring, while the circular and cantilever structures need micromachining to create the cavity. But the power consumption of planar structure is high because most of the heat disperses to substrate in this structure, only small portion of heat is used for creating temperature difference between hot and cold contacts.

Both the planar and cantilever test structures contain only a single polysilicon thermal leg, mostly it is difficult to stably measure the thermovoltage at small heating current, and then causes measurement error of Seebeck coefficient. In the circular test structure, the thermovoltage generated from the five pairs of thermocouples is ten times larger than the one from a single thermal leg. Therefore, the voltage reading is quite stable, which helps to reduce the measurement error. Unlike planar or cantilever structure, the proposed circular test structure can only measure average absolute Seebeck coefficient of n- and p-type polysilicon. However, if we change the metal routing in the circular structure, it is possible to measure individual type of polysilicon. Comparison of the presented three test structures of measuring Seebeck coefficient is summarized in Table 1.

4 Conclusions

Three test structures for extracting Seebeck coefficient of doped polysilicon are fabricated by CMOS compatible process. The circular test structure is a novel design which is firstly reported in this paper. To compare with the previously reported planar and cantilever test structures, all these three structures are fabricated together in one wafer so that the measured polysilicon samples are under the same process conditions. Working principle and measurement procedure for the three test structures are presented respectively. The measured Seebeck coefficients from circular and cantilever structures show a small error of 4%, while the result from planar structure is considered with an error about 14%. The circular test structure is a good choice for deriving the average absolute values of Seebeck coefficient of p-type and n-type. However, the planar test structure with advantage of simple fabrication process can allow the separate characterization of Seebeck coefficients of p-type or n-type polysilicon at moderate accuracy, while the cantilever test structure can provide accurate measurement results of Seebeck coefficients of p-type or n-type polysilicon separately.

Acknowledgments This work was supported by the Science and Engineering Research Council of A*STAR (Agency for Science, Technology and Research), Singapore.

References

Arx Mv, Paul O, Baltes H (1997) Test structures to measure the Seebeck coefficient of CMOS IC polysilicon. IEEE Trans Semiconductor Manuf 10:201–208

Arx Mv, Paul O, Baltes H (2000) Process-dependent thin-film thermal conductivities for thermal CMOS MEMS. J Microelectromech Syst 9:136–145

Baltes H, Paul O, Brand O (1998) Micromachined thermally based CMOS microsensors. Proc IEEE 86:1660–1678

Boutchich M, Ziouche K, Godts P, Leclercq D (2002) Characterization of phosphorus and boron heavily doped LPCVD polysilicon films in the temperature range 293–373 K. IEEE Electron Device Lett 23:139–141

Du CH, Lee C (2000) 3D Thermoelectric structures derived from a new mixed micromachining process. Jpn J Appl Phys 39: 7125–7129

Hirota M, Nakajima Y, Saito M, Uchiyama M (2007) 120 × 90 element thermoelectric infrared focal plane array with precisely patterned Au-black absorber. Sens Actuators A 135:146–151

Huang IY, Lin JC, She KD, Li MC, Chen JH, Kuo JS (2008) Development of low-cost micro-thermoelectric coolers utilizing MEMS technology. Sens Actuators A 148:176–185

Mancarella F, Roncaglia A, Cardinali GC (2006) A measurement technique for thermoelectric power of CMOS layers at the wafer level. Sens Actuators A 132:289–295

Socher E, Bochobza-Degani O, Nemirovsky Y (2000) Optimal performance of CMOS compatible IR thermoelectric sensors. J Microelectromech Syst 9:38–46

Strasser M, Aigner R, Lauterbach C, Sturm TF, Franosch M, Wachutka G (2004) Micromachined CMOS thermoelectric generators as on-chip power supply. Sens Actuators A 114:362–370

Wang Z, Fiorini P, Leonov V, Hoof CV (2009a) Characterization and optimization of polycrystalline Si70%Ge30% for surface micromachined thermopiles in human body applications. J Micromech Microeng 19:094011

Wang Z, Leonov V, Fiorini P, Hoof CV (2009b) Realization of a wearable miniaturized thermoelectric generator for human body applications. Sens Actuators A 156:95–102

Wijngaards DDL, Wolffenbuttel RF (2002) Thermo-electric characterization of APCVD polySi0.7Ge0.3 for IC-compatible fabrication of integrated lateral Peltier elements. IEEE Electron Device Lett 23:139–141

Xie J, Lee C, Wang M, Liu Y, Feng H (2009) Characterization of heavily doped polysilicon films for CMOS MEMS thermoelectric power generators. J Micromech Microeng 19:125029

Xie J, Lee C, Feng H (2010) Design, fabrication and characterization of CMOS MEMS based thermoelectric power generators. J Microelectromech Syst 19:317–324

Yang SM, Lee T, Jeng CA (2009) Development of a thermoelectric energy harvester with thermal isolation cavity by standard CMOS process. Sens Actuators A 153:244–250

Yang SM, Lee T, Cong TM (2010) Design and verification of a thermoelectric energy harvester with stacked polysilicon thermocouples by CMOS process. Sens Actuators A 157:258–266