Design, Fabrication, and Characterization of CMOS MEMS-Based Thermoelectric Power Generators

Jin Xie, Chengkuo Lee, and Hanhua Feng

***Abstract*—This paper presents the design, modeling, fabrication, and characterization of CMOS microelectromechanical-systems-based thermoelectric power generators (TPGs) to convert waste heat into a few microwatts of electrical power. Phosphorus and boron heavily doped polysilicon thin films are patterned and electrically connected to consist thermopiles in the TPGs. To optimize heat flux, the thermal legs are embedded between the top and bottom vacuum cavities, which are sealed on the wafer level at low temperature. A heat-sink layer is coated on the cold side of the device to effectively disperse heat from the cold side of the device to ambient air. The peripheral cavity is designed to isolate heat from the surrounding silicon substrate. Both simulation and experiments are implemented to validate that the energy conversion efficiency is highly improved due to the aforementioned three unique designs. The device has been fabricated by a CMOS-compatible process. Properties of thermoelectric material, such as the Seebeck coefficient, electrical resistivity, and specific contact resistance are measured through test structures. For a device in the size of 1 cm^2 and with a 5-K temperature difference across the two sides, the open-circuit voltage is 16.7 V and the output power is 1.3 μW under matched load resistance. Such energy can be efficiently accumulated as useful electricity over time and can prolong the battery life. [2009-0066]**

***Index Terms*—CMOS microelectromechanical systems (MEMS), energy harvester, power generator, thermoelectric, thermopile, vacuum.**

I. Introduction

ELECTRONIC devices traditionally employ batteries as power sources. However, for powering wireless sensor nodes and implanted medical devices, it is very difficult to replace batteries and such replacement cost is high. Moreover, the environmental impact of producing and disposing of chemical cells of commercial batteries is an increasingly pressing concern. Hence, there was a lookout for alternative technologies with high reliability and long life for powering the devices aforementioned. This demands the development of energy-harvesting technology. Compared with traditional batteries, energy harvesters have several advantages, such as compactness, environment friendliness, unlimited lifetime, and autonomy. As a kind of energy-harvesting device, thermoelectric power generators (TPGs) have been proposed to generate electricity from body heat or any environment where there is a temperature gradient. Currently, most commercial TPGs [1] use Bi_2Te_3 as thermoelectric material due to its large thermoelectric figure of merit. Researchers at IMEC [2] presented the first prototype of wireless sensor nodes on human beings powered by thermoelectric generators using Bi_2Te_3 material. MicroPelt [3] described the first thermoelectric devices based on the V–VI compounds Bi_2Te_3 and $(Bi, Sb)_2Te_3$ which can be manufactured by means of regular thin-film technology in combination with microsystem technology. However, Bi_2Te_3 and its alloy are still difficult to produce, and significant efforts are required to make the material compatible with well-established silicon thin-film processes. Furthermore, they are not CMOS-compatible materials, which means that Bi_2Te_3 material-based approaches cannot be monolithically integrated on microelectronics in normal CMOS manufacturing lines.

Large Seebeck effects are found in doped poly-Si, which makes it a promising choice for thermoelectric devices based on CMOS technology. With microelectromechanical systems (MEMS) technology, the thin film of poly-Si is deposited and patterned to form thermocouples, and an array of thermocouples, i.e., a thermopile, could be arranged in a tiny area. The key challenge of thin-film thermopiles is that the internal thermal resistance is very small compared with the thermal contacts of the surrounding assembly, so that the temperature difference between the two ends of a thermocouple is small. Because the output voltage of TPG is proportional to the temperature difference between two junctions of thermocouples, an appropriate heat flux path is necessary to be managed in order to obtain the largest temperature difference. Infineon demonstrated micromachined TPGs using thermocouples made of poly-Si or poly-SiGe and introduced a cavity into the substrate to force cross-plane heat to flow through the in-plane thermocouples [4], [5]. Because the thermal insulation on the front side of the device is not sufficient, the effective temperature difference between the two junctions of thermocouples is limited. On the other hand, the IMEC group developed TPGs based on poly-SiGe materials and with improved energy conversion efficiency by creating trenches under cold junctions and forming rim structures to match thermal resistance with ambient air [6]. A device with a similar trench structure realized by wafer bonding is reported by [7], in which the authors fabricated n-poly-Si/Al thermopiles and covered the device surface with metal as a thermal contact pad to help optimize the heat flux. Lee *et al.* [8] also investigated a design of CMOS MEMS-based TPGs with

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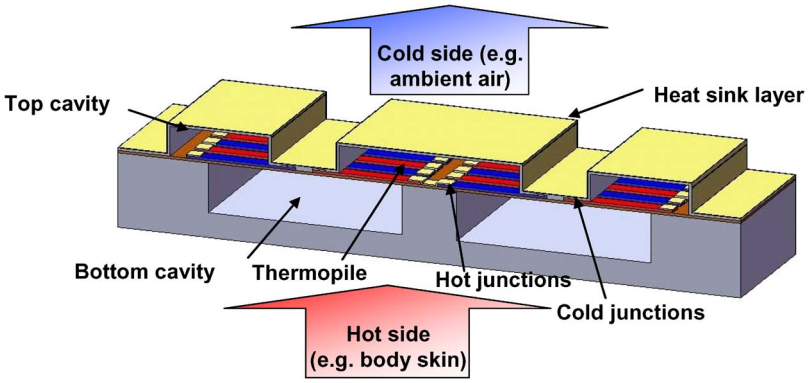


Fig. 1. Schematic view of the proposed TPG.

wafer-bonded vacuum cavities on both sides of a suspended thermoelectric membrane. As we can see, the vacuum cavity has become an effective approach to increase the performance of TPGs. Recently, researchers have proposed technologies for low-temperature wafer-level sealing technology for creating sealed vacuum cavities. For example, Stark and Najafi [9] demonstrated wafer-level sealed vacuum cavities by using electroplated thick nickel films, and P. Monajemi *et al.* [10] presented a low-temperature packaging technique which utilizes the decomposition of a sacrificial polymer through a gas-permeable polymer overcoat. However, these technologies are so-called post-CMOS processes, and materials are not available in the standard CMOS manufacturing line. Thus, making a TPG with vacuum cavities which are sealed by low-cost and low-temperature wafer-level technology based on CMOS materials and processes becomes an interesting research subject to us.

This paper presents a novel micromachined TPG that matches the needs of low cost, small size, and improved energy conversion efficiency. The thermocouples are embedded between two microscale vacuum cavities, which are sealed at a temperature that aluminum can stand, i.e., not higher than 400 °C. The two vacuum cavities can effectively avoid heat loss via ambient air and underneath substrate and then maximize the temperature difference between hot and cold junctions. The overcoat metal layer on top of vacuum cavities plays the role of a heat sink, which helps disperse heat from cold junctions to the ambient air. In addition, a peripheral cavity is designed around the device area to reduce heat loss from the silicon substrate. With these three unique designs, outstanding energy conversion efficiency is achieved. More importantly, the proposed power generator is fabricated by a CMOS-compatible process, which allows us to realize a novel on-chip power source to enable self-powered CMOS IC and MEMS devices.

II. Theory, Design, and Modeling

According to the Seebeck effect, the open-circuit output voltage U_o is given by

$$U_o = m\alpha\Delta T_G \tag{1}$$

where m is the number of thermocouples, α is the relative Seebeck coefficient, i.e., the absolute difference of the Seebeck coefficient of the n-doped poly-Si and p-doped poly-Si, and ΔT_G is the temperature difference between the hot and cold junctions. The output power P_o is given by (2) and is achieved under matched load resistance, i.e., the internal resistance of the generator R_G is equal to the load resistance connected to the generator

$$P_o = U_{\text{out}} I = \frac{U_o^2}{4R_G} = \frac{m^2\alpha^2}{4R_G}\Delta T_G^2 \tag{2}$$

where U_{out} is the output voltage under load and I is the electrical current. If the heat contributions by the Peltier effect and Joule heat are neglected, ΔT_G is simply expressed as

$$\Delta T_G = \frac{K_G}{K_G + K_C + K_H}\Delta T \tag{3}$$

where K_C and K_H are the thermal resistance at the cold and hot sides, respectively, and ΔT is the temperature difference over the two sides of the device. If the Peltier effect and Joule heat are included, the expression of ΔT_G is more complicated, as given in [5]. In order to compare the performance of different thermoelectric generators, a figure φ, which is called power efficiency factor [11], is defined as

$$\varphi = \frac{P_0}{A_G \Delta T^2} \tag{4}$$

where A_G is the surface area. The power efficiency factor needs to be maximized by optimizing the dimension of the thermal leg.

The proposed power generator is shown in Fig. 1. Planar thermopiles are arranged on top of the substrate due to the limited thickness of the thermoelectric material by thin-film technology. Since heat transfers cross the device from bottom side to top side, to obtain a large temperature difference between the two junctions of the thermocouple, the heat must be redirected to flow along the longitudinal direction of thermal legs. Designs of the bottom cavity to guide heat flux have been seen in several reported TPGs [4]–[7]. However, in these devices, few efforts were made to reduce thermal insulation from the top side and avoid the hot junctions cooled by ambient air. Heat loss by air convection from the top side is even heavier when the device surface has a high convection coefficient. For example, the TPG moves with the body during walking or sporting when it is worn on the wrist. In the proposed TPG, a novel dual-cavity structure is first introduced to optimize heat flux. Each

TABLE I
THERMAL CONDUCTIVITY OF MATERIAL USED IN FEA SIMULATION

	Poly-Si	Silicon	SiO_2	Si_3N_4	Al	Air
Thermal conductivity (W/mK)	31.4 [5]	149 [12]	1.25 [12]	15.0 [12]	237.0 [12]	0.35[13],[a]

[a] Effective thermal conductivity, including conduction, convection and radiation

thermal leg is embedded between the bottom and top cavities. The bottom cavities are created on the wafer level to guide the heat flux through thermal legs, as aforementioned, while the top cavities protect hot junctions from being cooled by air convection. In contrast, the area of cold junctions is exposed to ambient air. Both the bottom and top cavities are sealed with high vacuum levels to minimize heat loss due to heat conduction and convection through air. With such a design, the planar thermopiles work like a vertical configuration. Second, a thin metal layer covers the top surface of the device as a heat sink, i.e., a heat dissipation layer. This metal layer covers the whole device area such that the whole device area is supposed to be able to release heat to ambient air effectively. It makes the heat easily disperse from the cold sides to air and then enlarges the temperature difference across the device.

A 3-D model is built with the software ANSYS for thermal finite-element analysis (FEA). The thermal conductivity of each material used in simulation is shown in Table I. A fixed temperature difference of 5 K between the top and bottom of the device is assumed as boundary conditions for thermal analysis. The optimized parameters of the generator model have been determined by varying the length, width, and thickness of the thermal legs. The variable to be maximized is the power efficiency factor, as shown in (4). The optimization is done based on the average thermal and electrical conductivities for p- and n-thermal legs. For a layer thickness of 0.7 μm, an optimum is found for thermal legs of 16-μm effective length and 5-μm width. According to this dimension, 31 536 thermocouples could be arranged in a chip with a size of 5×5 mm^2. To validate the improvement achieved by having vacuum cavities, power generators with air or vacuum cavities are simulated, respectively. For the design with top and bottom vacuum cavities, the temperature difference ΔT_G between hot and cold junctions is 3.75 K, as shown in Fig. 2(a). However, for the design with air cavities, the temperature difference ΔT_G is derived as only 2.77 K when heat loss due to air conduction and convection is considered, as shown in Fig. 2(b). According to (2), output power is a second-order function of ΔT_G; therefore, the output power is improved by about 83% based on the design with top and bottom vacuum cavities.

In those conventional designs of TPGs, only the heat transfer from the bottom side to the top side is considered. However, because the silicon substrate is of high thermal conductivity, for the thermocouples located at the rim edge of the device region, the temperature of the surrounding silicon frame is higher than that at cold junctions, which causes a small part of heat transfer from the surrounding silicon to the cold junctions. The cold junctions of these thermocouples are heated up, and then, the temperature differences between the hot and cold junctions are reduced. In our device, peripheral cavities (not shown in Fig. 1) are created around the device edge region to isolate heat from

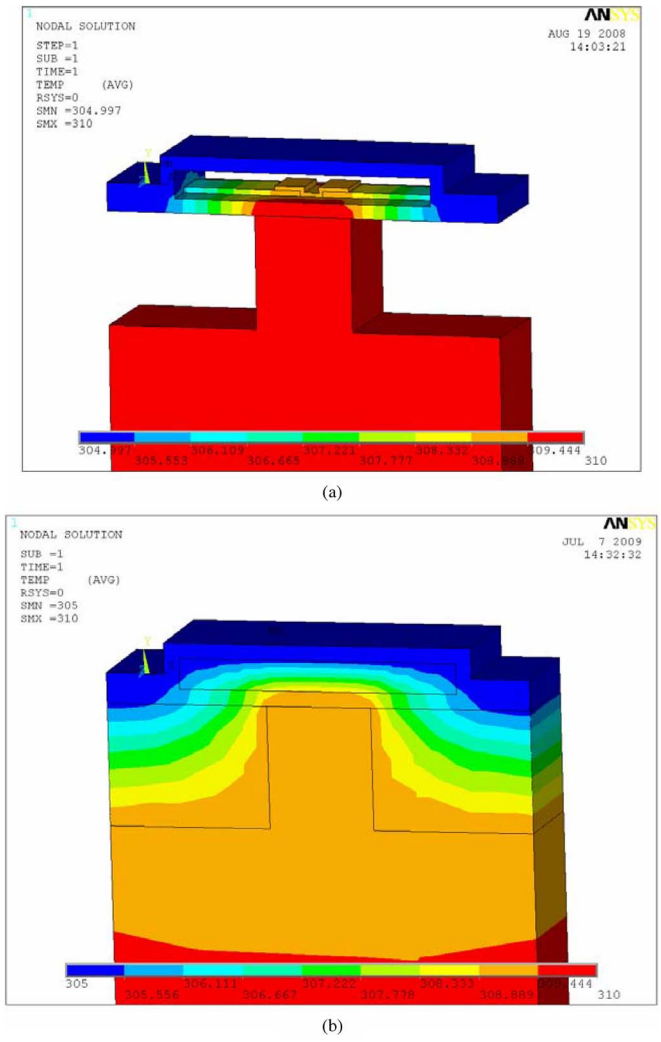
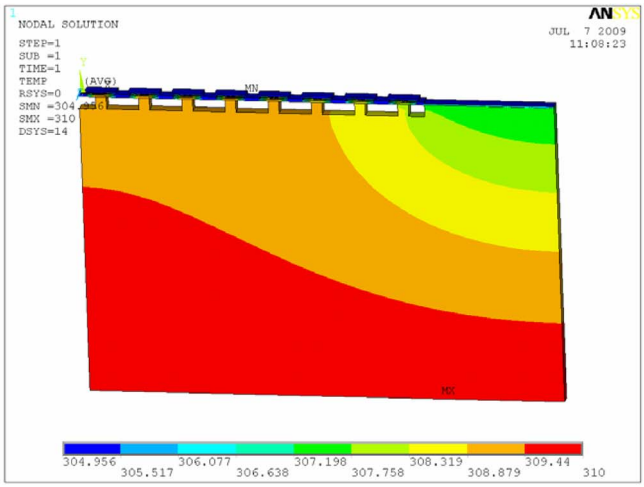
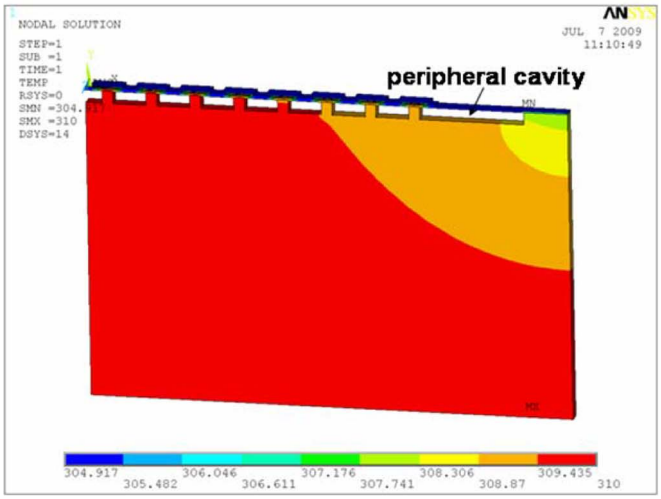


Fig. 2. FEA result for (a) design with top and bottom vacuum cavities, $\Delta T_G = 3.75$ K, and (b) design with bottom top and bottom air cavities, $\Delta T_G = 2.77$ K. (The thermal legs are covered by the air element).

the surrounding silicon substrate, so that the performance of those thermocouples at the rim of device region is not affected by the heat from the surrounding silicon substrate. To consider this effect, a finite-element model for the eight elements of the thermocouples as well as the surrounding silicon substrate is built and analyzed. From the result of the thermal analysis, as shown in Fig. 3, it is found that a ΔT_G close to the surrounding silicon is obviously limited by the surrounding silicon. The closer the thermocouple to the surrounding silicon, the lower the ΔT_G. Taking the average value of ΔT_G for the eight thermocouples, it is found that ΔT_G is reduced to 3.02 K, as shown in Fig. 3(a). To cut off the heat transferring from the surrounding silicon, we proposed to enlarge the peripheral cavity around the device edge rim area. The peripheral cavity is 80 μm in width and 30 μm in depth. The peripheral cavity is completely sealed with a thin silicon oxide film; therefore, the thermal resistance is high enough to resist the heat coming from the surrounding silicon. From the FEA result, the average ΔT_G is observed as 3.56 K in Fig. 3(b). It points out that the output power is further improved by about 39% compared with the design without peripheral cavity, i.e., Fig. 3(a).



(a)



(b)

Fig. 3. FEA result for the device (a) without peripheral cavity, average $\Delta T_G = 3.02$ K, and (b) with peripheral cavity, average $\Delta T_G = 3.56$ K.

III. Fabrication

In this section, we report the CMOS-compatible process for making the proposed TPG. The main process steps are shown in Fig. 4(a)–(g). The 0.7-μm-thick poly-Si as thermoelectric layer is deposited at 580 °C in furnace by low-pressure chemical vapor deposition. Then, the poly-Si layer is dry etched to form thermoelectric leg patterns with 5 μm in width and 16 μm in length [Fig. 4(a)]. Afterwards, the poly-Si layer is partially phosphorus-implanted with 180-keV energy to generate the n-type thermoelectric legs and is subsequently boron-implanted using 80 keV in the other half region to form the p-type thermoelectric legs. A doping dose of 10^{16} cm^{-2} is used in both steps. The doped poly-Si is annealed in furnace at 1000 °C for 30 min. After SiO_2 insulating layer depositing and contact via opening, an aluminum layer is deposited and etched to form electrical interconnects between the p- and n-type thermoelectric legs in series, as shown in Figs. 4(b) and 5(a), respectively. To establish the better electrical contact between the Al and polysilicon, the wafer is annealed at 420 °C for 30 min and is then passivated by a Si_3N_4 layer [Fig. 4(b)]. In order to optimize the heat flux direction within the TPG, bottom and top vacuum cavities are created. In the micromachining step shown in Fig. 4(c), a 0.2-μm-thick SiO_2 hard mask is patterned with openings first. Si trenches with depths of 15 μm are etched into the silicon substrate by deep reactive ion etching (DRIE) based on SF_6 and C_4F_8 gases, and then, the wafer is isotropically etched by SF_6 to remove the silicon between the trenches and to create the bottom cavities [Fig. 4(c)]. The top view of the TPG device at this step is shown in Fig. 5(b). Then, the bottom cavities are sealed by a 3-μm-thick low-stress undoped silicate glass (USG) layer which is deposited by plasma-enhanced chemical vapor deposition (PECVD) at 400 °C. The sealed vacuum in the cavities is considered to be the same as the process pressure in the PECVD reaction chamber, i.e., 2.4 torr. In addition, a 150-nm-thick amorphous silicon layer is deposited to protect the SiO_2 of the sealing layer from the buffered oxide etchant (BOE) etching in the later step, as shown in Fig. 4(d).

To create the top vacuum cavity, the wafer starts with a 2-μm patterned USG as a sacrificial layer and is covered by a 700-nm PECVD Si_3N_4 and 200-nm amorphous silicon. Small etching holes of 1-μm width and 3-μm length are etched through nitride and amorphous silicon layers [Fig. 4(e)]. Thereafter, the wafer is dipped in the BOE for about 20 min in order to remove the sacrificial layer of USG via the etching holes. In the step in Fig. 4(f), the holes are again sealed by a 2.5-μm-thick low-stress USG in the PECVD reaction chamber. The top view of the fully sealed surface of the TPG is shown in Fig. 5(c). At this step, there is an oxide layer that is about 5.5 μm thick accumulated on top of the cold junctions. To make the cold junctions cooled easier by ambient air, this thick oxide covering the cold junctions is etched after another photolithography and etching step, and only a 1-μm-thick oxide is retained as insulation layer. Finally, a 0.7-μm-thick aluminum is deposited to cover the whole device area as the heat-sink layer [Fig. 4(g)]. The top view of the TPG with sealed top cavities is shown in Fig. 5(d). Fig. 6(a) shows the top view of a one-element TPG. Several TPG elements can be selected to form a TPG device with the dimension demanded by particular applications. Fig. 6(b) shows the cross section of two thermocouples, from which each layer of the TPG can be seen. The sealed bottom cavity is about 30 μm in depth and 42 μm in width, while the encapsulated top cavity is 2 μm in height and 35 μm in width, and the lengths of both bottom and top cavities are about 670 μm.

IV. Characterizations

The properties of the thermoelectric material including the Seebeck coefficient, sheet resistance, and specific contact resistance have been measured and listed in Table II. The Seebeck coefficient is measured by using a special planar test structure [14]. Through measuring the temperature difference and voltage of two ends of a 670-μm-long and 30-μm-wide planar poly-Si strip, the Seebeck coefficient can be calculated. The experimental result shows that thermoelectric coefficient value is 279 μV/K at room temperature, because a thermocouple is made of n- and p-type thermocouples with thermoelectric coefficients of -132 μV/K for n-type and 147 μV/K for p-type, respectively. The electrical resistivity is determined by using the van der Pauw structure and is derived as 2.786×10^{-5} $\Omega \cdot$ m

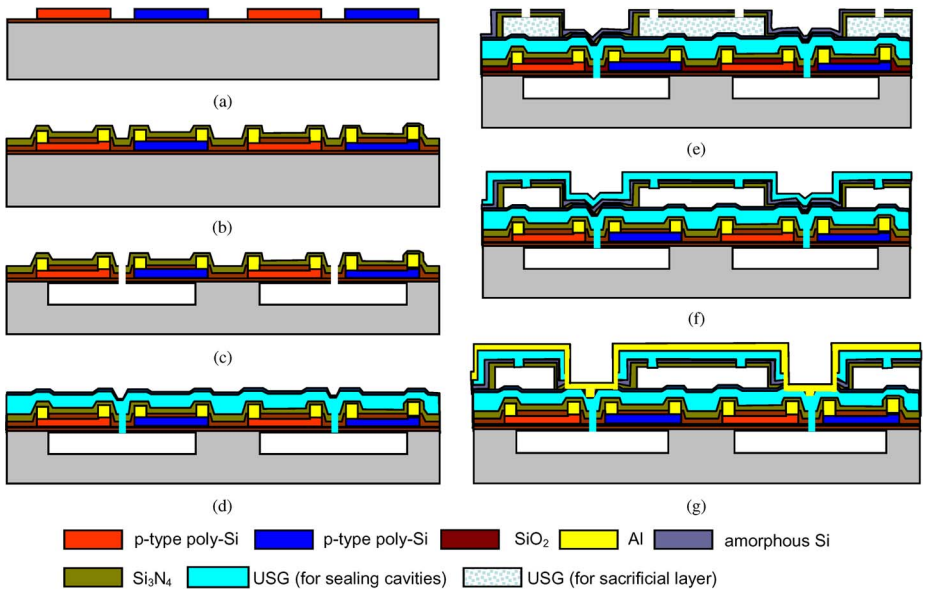


Fig. 4. Fabrication process of power generator. (a) Patterning and doping poly-Si. (b) Metal junctions and Si_3N_4 passivation layer. (c) Perforating holes, DRIE, and isotropic etching silicon. (d) Sealing bottom cavities. (e) Patterning USG sacrificial layer and opening etching holes. (f) Removing USG sacrificial layer and sealing the top cavities. (g) Partially etching oxide at area of cold junctions and coating metal on whole device.

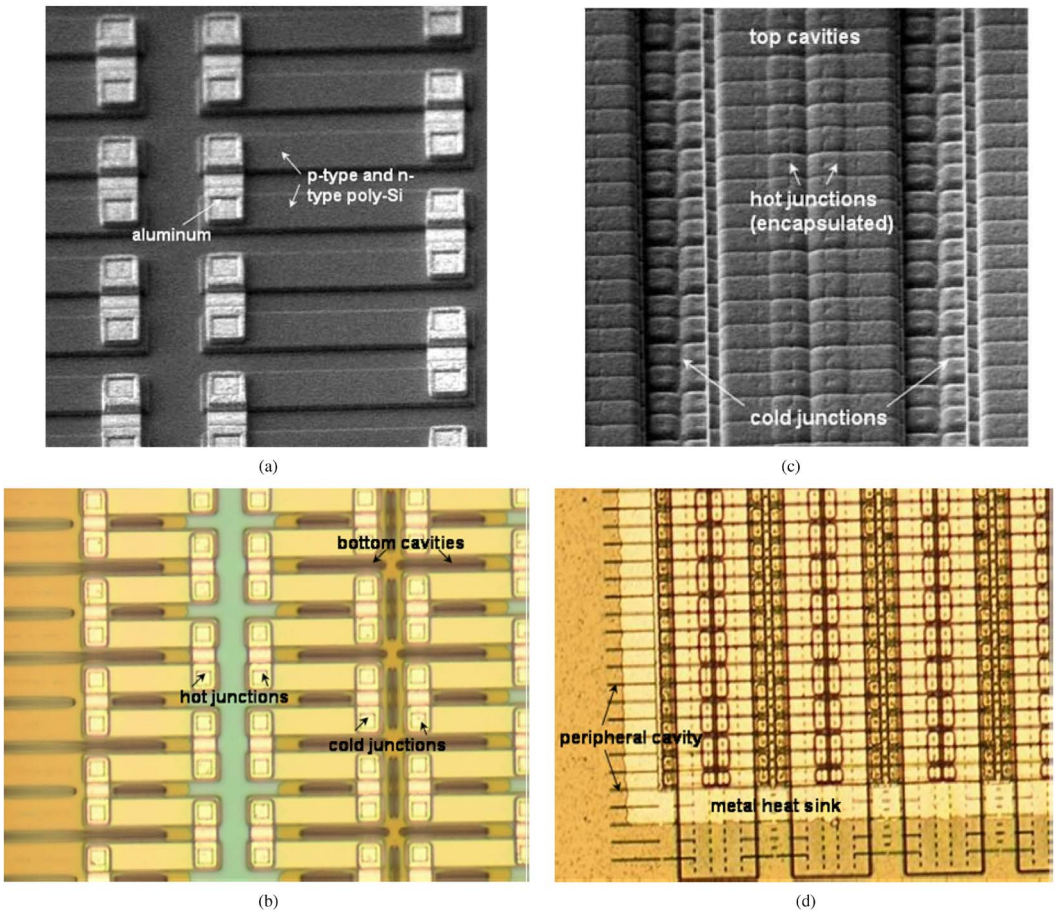
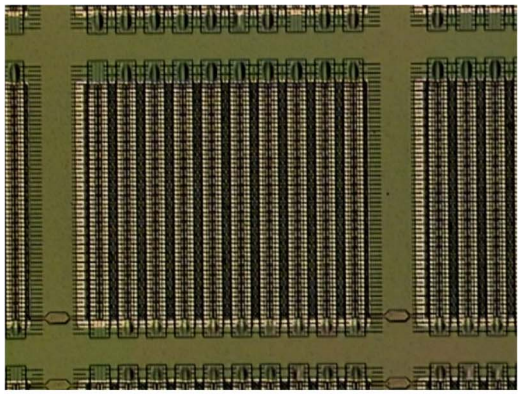
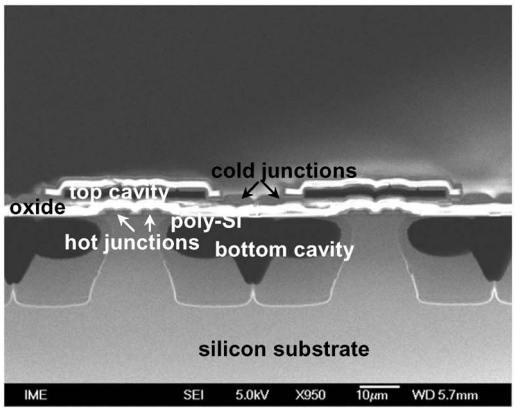


Fig. 5. SEM and microscopic images of TPG in different stages of fabrication. (a) Patterned and electrically connected poly-Si. (b) Created bottom cavities: Shadowed areas indicate the region of bottom cavities. (c) Sealed top cavities. (d) Heat-sink Al metal layer deposition.

for p-type and $1.932 \times 10^{-5}\ \Omega \cdot \mathrm{m}$ for n-type poly-Si. By using Kelvin structures, the specific electrical contact resistance is found to be 360 and 477 $\Omega \cdot \mu\mathrm{m}^2$ for the contacts of metal to the p- and n-type polysilicon. Thermal conductivity can be referred to the reported data [5], in which it is about 31 $\mathrm{W} \cdot \mathrm{m}^{-1} \cdot \mathrm{K}^{-1}$ for poly-Si with a doping dose of $10^{16}\ \mathrm{cm}^{-2}$.



(a)



(b)

Fig. 6. (a) Microscopic image of the top view of the TPG after completed fabrication. (b) SEM photograph of the cross-sectional view of the TPG.

TABLE II
MEASURED MATERIAL PROPERTIES OF 700-nm-THICK POLY-SI LAYERS AFTER BORON AND PHOSPHORUS DOPING WITH DOSE OF 10^{16} cm^{-2}

Material	Seebeck coefficient α (μVK^{-1})	Electrical resistivity ρ (Ωm)	Specific contact resistance R_c ($\Omega\mu$m^2)
p-poly-Si	147	2.786×10^{-5}	360
n-poly-Si	-132	1.932×10^{-5}	477

The device chips under test are diced into 1 cm $\times$ 1 cm sizes. It includes 125 144 thermocouples which equals to four TPG elements, as shown in Fig. 7. The measurement setup is shown in Fig. 8. The device under test is placed between a hot plate and a brass heat sink, which is cooled by a commercial Pelteir cooler. A CPU fan is mounted to disperse heat from the cooler to ambient air. Two PT100 temperature sensors are integrated into the hot plate and heat spreader for sensing temperature. The temperature difference and range can be adjusted via two PID controller units driving the hot plate and the Peltier cooler, separately. A Hewlett Packard 34401A digital multimeter is used to record the internal resistance and output voltage. The temperature difference across the generator ΔT is limited due to the thermal contact resistance K'_C between the heat sink and the TPG and to the K'_H between the hot plate and the TPG. The temperature difference $\Delta T_{\rm meas}$ is measured via the two temperature sensors. The actual temperature difference ΔT across the TPG is unknown, but it can be estimated by FEA as we know the geometry and material parameters of the setup

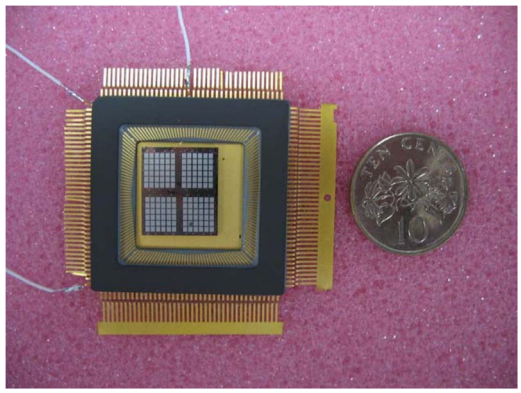


Fig. 7. TPG prototype assembled in ceramic package and placed beside a Singapore ten-cent coin.

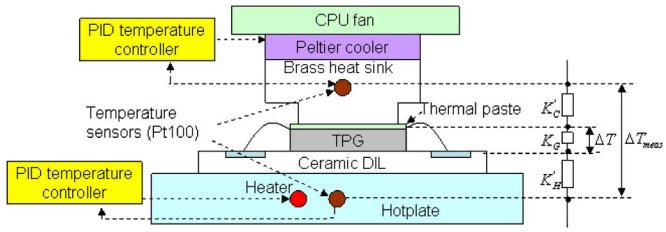


Fig. 8. Schematic of testing setup.

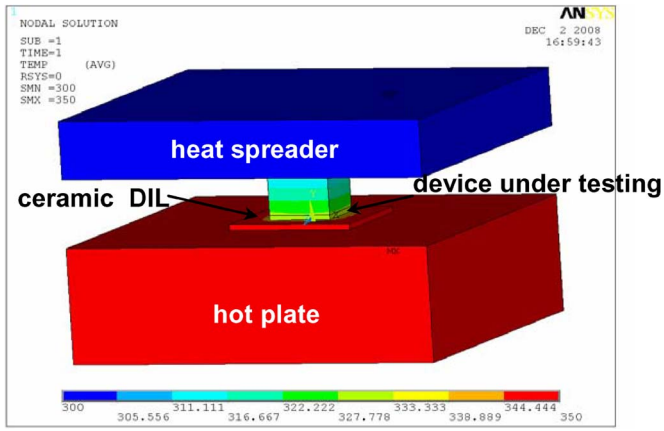


Fig. 9. FEA result of the ratio of the thermal resistance of the testing setup and the device chip.

and the device. A finite-element model is built for the whole setup, such as the brass heat spreader, thermal paste, device, DIL (made of ceramic), and hot plate, as shown in Fig. 9. When a 50-K temperature difference $\Delta T_{\rm meas}$ is created and measured by the two temperature sensors, a ΔT of 1.92 K is observed across the TPG chip. Thus, the temperature difference across the chip, i.e., ΔT, is reduced to only 3.84% of the externally measured value $\Delta T_{\rm meas}$.

The internal resistance of the generator with a size of 1 cm $\times$ 1 cm is 52.8 MΩ, where 23 MΩ comes from the contact resistance of vias between the poly-Si and metal. Thus, the contact resistance occupies about 43.6% of the total internal resistance. The open-circuit voltage is a linear function of the temperature difference across the device, as shown in Fig. 10. The output power per area versus temperature difference under matched load resistance is shown in Fig. 11. It is found that, when a 5-K difference is maintained across the two sides of the

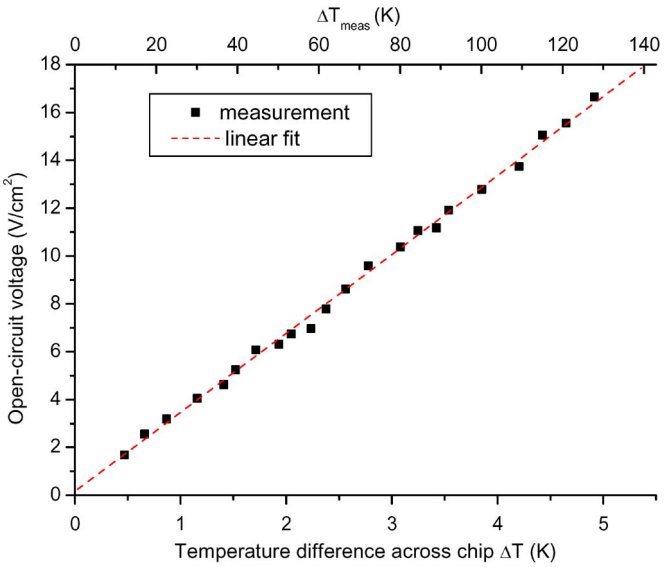


Fig. 10. Open-circuit voltage versus temperature difference across chip.

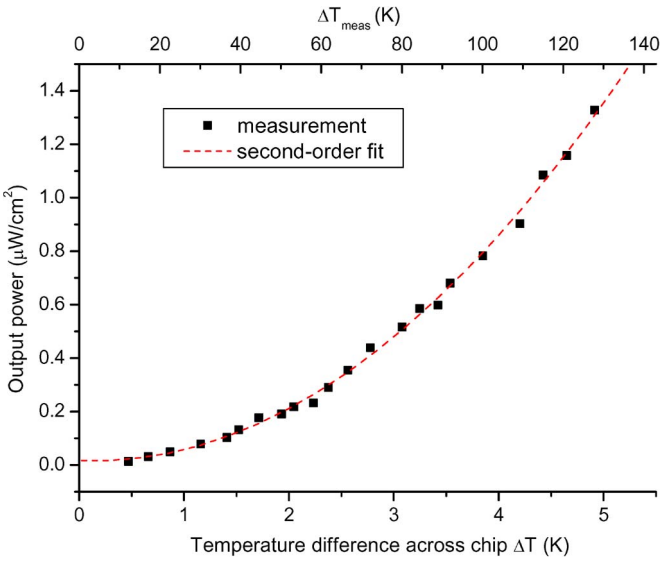


Fig. 11. Output power versus temperature difference across chip.

device (1 cm $\times$ 1 cm), the open-circuit voltage is 16.7 V, and the derived output power is 1.3 μW/cm^2. The power efficiency factor φ of the fabricated TPG is 0.052 μW/cm$^{-2} \cdot$ K^{-2}. For the previously reported TPGs fabricated based on a CMOS-compatible process, the power efficiency factor is 0.0352 μW/cm$^{-2} \cdot$ K^{-2} for Infineon's device [5], and it is 0.016 μW/cm$^{-2} \cdot$ K^{-2} for the device reported by the University of Freiburg [7]. One key feature for us to improve in the future is to reduce the contact resistance by adding a nickel silicide layer between poly-Si and aluminum. It is expected that the contact resistance could be reduced to about one quarter of the currently presented value. Therefore, the output power will accordingly increase about 48%, i.e., about 1.9 μW, for a chip with a size of 1 cm^2 with a 5-K temperature difference across the two sides of the device.

In most practical applications, the top side of the TPG is expected to be naturally cooled by ambient air instead of being forcedly cooled by a Peltier cooler. For example, when the generator is attached on the body skin to harvest body heat, the cold side of the TPG is preferred to be naturally cooled by ambient air. Therefore, another testing is implemented to evaluate the performance of the TPG without forced cooling. In this testing, the device is placed on the hot plate, while there is no Peltier cooler on the top side. The temperature difference is calculated from the measured temperature of the hot plate and ambient air. As shown in Fig. 12, for a chip with a size of 1 cm $\times$ 1 cm, the open-circuit voltage is derived as 480 mV at a temperature difference of 30 K. This result is close to the reported data from IMEC [6], i.e., the open-circuit voltage was 160 mV at a 50-K temperature difference for a chip with size of 4 mm $\times$ 4 mm.

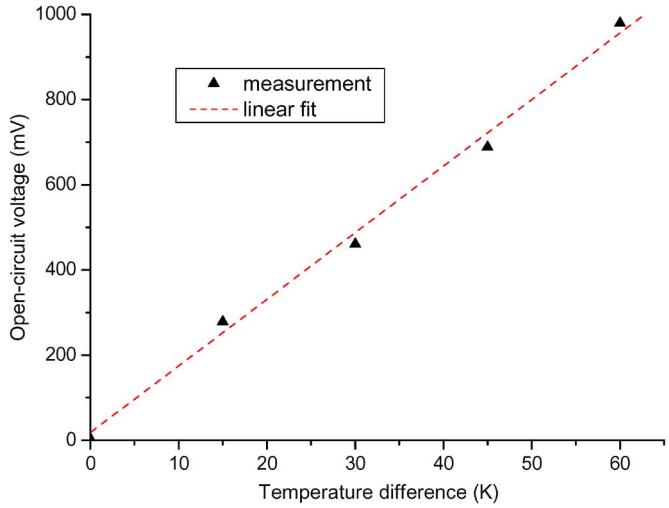


Fig. 12. Open-circuit voltage versus temperature difference when it is naturally cooled by ambient air.

Generally speaking, the measured open-circuit voltage is relatively smaller than the data measured by a forced cooling approach, mainly because the air around the bottom hot plate is heated so that the actual temperature difference between the hot plate and ambient air is far smaller than the one used for calculation. Therefore, in the naturally cooling case, the output power from the TPG is in the nanowatt range due to the small open-circuit voltage and large internal electrical resistance. In conjunction with a battery or a supercapacitor, the proposed CMOS-compatible TPG may be used to extend the battery life. With further improvement in the thermal isolation engineering, the actual temperature difference in the next generation of TPGs may be enhanced so that power is generated in the microwatt range. Such novel TPG devices with output power in the microwatt range trap increasing interests for the realization of self-powered CMOS electronics of ultralow power consumption. Based on our approach, the CMOS-compatible TPG can be monolithically integrated with low-power CMOS circuits to form self-powered CMOS devices. Additionally, microsystems of low power consumption can be realized, too.

V. Conclusion

A novel CMOS MEMS-based TPG was designed and fabricated by a CMOS-compatible process. Three unique features are included in the proposed generator. First, top and bottom

vacuum cavities are created to manage the heat flow and maximize the temperature difference between the two junctions of the thermocouples. Second, a heat-sink layer is coated on the cold side of the device to effectively disperse heat from the cold side of the device to ambient air. Third, a peripheral cavity is designed to cut off heat from the surrounding silicon substrate, so that cold junctions of thermocouples at the rim edge of the TPG device area are not affected by the heat coming from the surrounding silicon. Both simulations and experiments are implemented to confirm that the energy conversion efficiency is highly improved based on the aforementioned three unique features. When a 5-K temperature difference is maintained across the two sides of a device with a size of 1 cm $\times$ 1 cm, the open-circuit voltage is 16.7 V and output power is 1.3 μW under matched load resistance. The power efficiency factor φ of the fabricated generator is calculated as 0.052 $\mu\text{W/cm}^{-2} \cdot \text{K}^{-2}$. Further improvement may enable the novel TPG to generate power in the microwatt range under naturally cooling conditions. Such energy can be efficiently accumulated as useful electricity over time and can prolong the battery life.

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