Wafer-Level Hermetic Bonding Using Sn/In and Cu/Ti/Au Metallization

Da-Quan Yu, *Member, IEEE*, Li Ling Yan, Chengkuo Lee, *Member, IEEE*, Won Kyoung Choi, Serene Thew, Chin Keng Foo, and John H. Lau, *Fellow, IEEE*

***Abstract*—Low-temperature hermetic wafer bonding using In/Sn interlayer and Cu/Ti/Au metallization was investigated for microelectromechanical systems packaging application. In this case, the thin Ti layer was used as a buffer layer to prevent the diffusion between solder interlayer and Cu after deposition and to save more solders for diffusion bonding process. Bonding was performed in a wafer bonder at 180 and 150 °C for 20 min with a pressure of 5.5 MPa. It was found that bonding at 180 °C voids free seal joints composed of high-temperature intermetallic compounds were obtained with good hermeticity. However, with bonding at 150 °C, voids were generated along the seal joint, which caused poor hermeticity compared with that bonded at 180 °C. After four types of reliability tests—pressure cooker test, high humidity storage, high-temperature storage, and temperature cycling test—dies bonded at 180 °C showed good reliability properties evidenced by hermeticity test and shear tests. Results presented here prove that high-yield and low-temperature hermetic bonding using Sn/In/Cu metallization with thin Ti buffer layer can be achieved.**

***Index Terms*—Hermeticity, In-Sn, microelectromechanical systems (MEMS), reliability, wafer bonding, wafer-level packaging.**

I. Introduction

BECAUSE microelectromechanical systems (MEMS) packaging technologies remain as application-specific solutions, the packaging of MEMS devices is one of the most challenge tasks of MEMS commercialization [1], [2]. The MEMS manufacturing process is a major driving force for low-temperature wafer bonding since the specific system requires the combination of different materials. Low-temperature fluxless bonding offers comparative advantages such as low residual stress and better process compatibility with devices for MEMS and BioMEMS application [3].

There are several kinds of wafer bonding methods for wafer-level packaging (WLP) such as direct (fusion) bonding, anodic bonding, and intermediate-layer bonding [4]. Anodic bonding is restricted to bond the glass with silicon, and standard silicon fusion bonding requires a high-temperature annealing step, which is the main limiting factor. Recently, low-temperature direct bonding was developed by special surface treatment techniques such as plasma surface treatment and chemical activation [3]. The choice of the intermediate-layer bonding is more flexible and can be decided by the type of substrates to be bonded. For intermediate-layer bonding, solders, adhesives and glass can be used. Although adhesive bonding and glass frit bonding are ready for low-temperature process, they have the problems of outgassing and contaminations. Nowadays, eutectic wafer bonding is used widely in WLP. Researchers have investigated several systems of low-temperature solders and high-melting-point parts [4]–[9]. Considering the bonding temperatures, formation of void-free joints, and reliable intermetallic compounds (IMC), Sn/Au and In/Au systems are studied extensively and are commonly used [4]–[6]. Among the low-temperature solder alloys, In-Sn alloy is a very attractive material due to its low eutectic temperature. As shown in Fig. 1, the composition of the eutectic (118 °C) point is 51.7 at% In and 48.3 at% Sn. The eutectic composition is composed of two intermediate-phase In-rich β and Sn-rich γ [10]. For the high-melting-point component for eutectic bonding, Cu is a very good candidate since it is widely used in modern packaging technology, and at the same time it is much cheaper and is wettable with various solders [8], [9]. Therefore we selected Sn/In/Cu metallization for wafer-level hermetic bonding.

Usually, for wafer-level hermetic eutectic bonding, the thickness of the solders and high-temperature component is about several micrometers. Therefore, one big challenge comes from the total thickness variations caused by the wafer warpage and materials deposition, which will be much more severe with increase of the wafer size. As a remedy, sufficient solder is required to reduce the effect of the nonplanarity issue. Previously, we have found the fast diffusion between low-temperature solders and Au/Cu metallization after solder deposition and relative dry film stripping process, and the formation of high-temperature phases, caused the low yield of good dies after wafer bonding [11]. The result indicated that when solders are directly put on the high-melting-point component, diffusion control should be employed to prevent fast diffusion during fabrication process and room-temperature storage.

For this reason, we introduced a thin Ni buffer layer into the high-melting-point components. The Ni buffer layer was used to prevent fast diffusion between Sn-In and Cu before bonding. Since the Ni layer was thinner, it was easily resolved into solder alloy, which allows the interdiffusion between solder and high-temperature component under bonding temperature. Using Ni buffer layer, we have successfully achieved high-yield hermetic wafer-level bonding using In-Sn with respect to Cu metallization system at 180 °C [11], [12].

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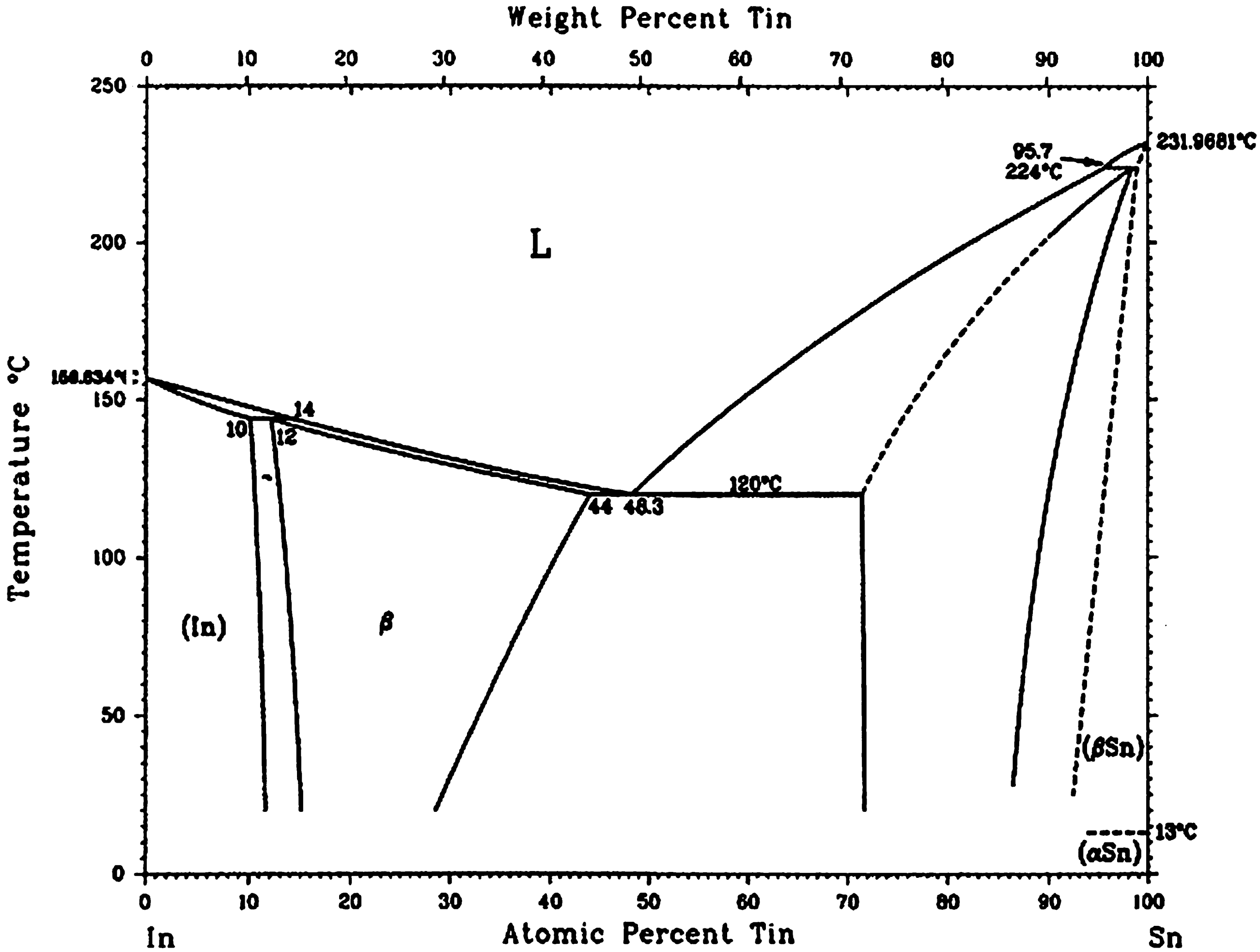

Fig. 1. Phase diagram of In-Sn alloy.

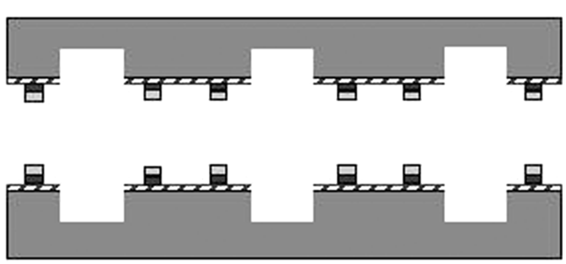

Fig. 2. Schematic view of top wafer and bottom wafer for bonding.

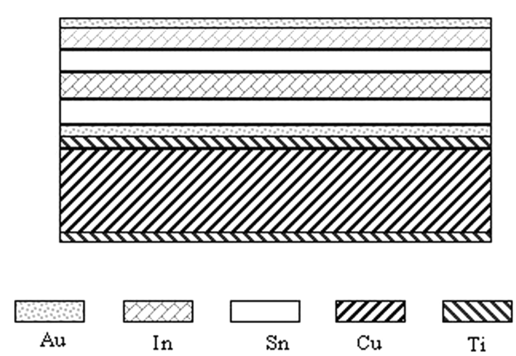

Fig. 3. Schematic of metallization deposited on wafers for low-temperature bonding.

Comparing with Ni, Ti is another kind of buffer layer that is a more effective barrier layer and more difficult to dissolve into liquid In-Sn solder [13], [14]. For a thin porous sputtered Ti layer, liquid solders may easily pass through the buffer-layer diffusion bonding. Therefore, it is interesting to explore the effect of such kind of buffer layer on the wafer-level bonding. In the research reported in this paper, the bonding quality, microstructure, and reliability properties using Ti buffer layer were investigated.

II. Experimental

Eight-inch wafers were used for present wafer bonding process. One hundred nineteen square seal rings with a size of 11×11 mm^2 and a width of 300 μm were designed and fabricated. At first, 300-Å-thick SiO_2 and 1500-Å SiN were formed on silicon wafer in turn by the thermal oxidation and low-pressure chemical vapor deposition process. They acted as hard mask for cavity etching. The patterning process was done by photolithography using dry film as a photoresist material. A cavity with an area of 6×6 mm^2 and 250 μm in depth was formed using a wet-etching process with KOH inside of each bonding ring on both the cap wafer and the bottom wafer.

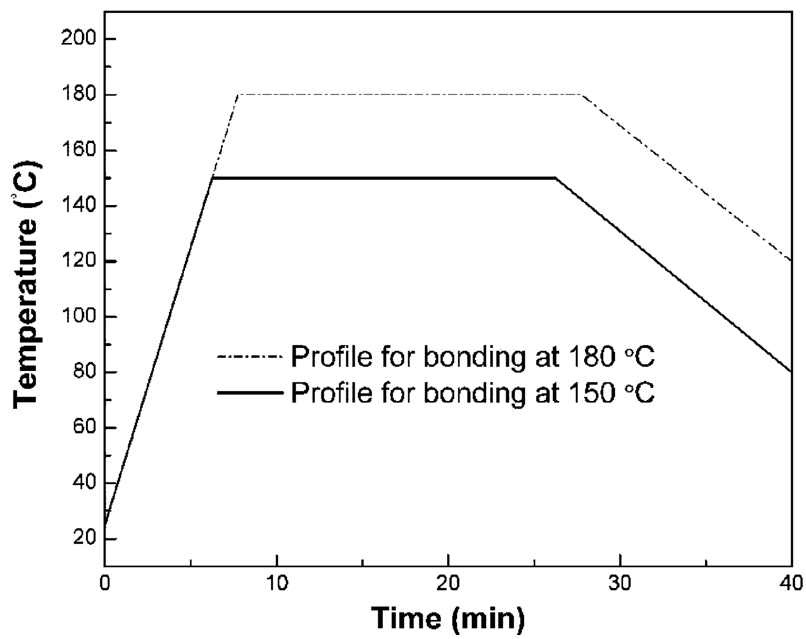

Fig. 4. Temperature profiles for wafer bonding at 180 and 150 °C.

The seal rings were constructed by Sn/In solder on Cu-based high-temperature components. Ti-Cu-Ti-Au metallization with a thickness of 0.05, 2, 0.05, and 0.03 μm was sputtered on $Si/SiO_2/SiN$ substrate. Here, the first thin Ti layer acted as the adhesive layer and the second Ti layer was the buffer layer. A thin Au layer was necessary for wetting and to prevent metals from oxidizing before solder deposition. For solder alloy, in order to achieve low-temperature In-Sn alloy in a relative short time, four layers of Sn/In/Sn/In solders were deposited with a thickness of 1, 1, 0.7, and 0.8 μm, respectively. According to this design, the atom percentage of Sn in In-Sn is about 50%, which is approximate to the eutectic composition of In-Sn alloy. Lastly, a 0.03 μm thin Au layer was deposited on the top to prevent oxidation during further process and storage. Fig. 2 shows the schematic view of top wafer and bottom wafer for bonding. The detail schematic of metallization deposited on wafers is shown in Fig. 3. After materials deposition and dry film strip, O_2 plasma descum was conducted before the bonding process to remove the oxide layer and organic contaminants.

The bonding was conducted in controlled N_2 atmosphere using wafer bonder (EVG520) with a pressure of 5.5 MPa upon the solder patterning area. In the work reported in this paper, the two bonded wafers were heated to a peak temperature of 180 and 150 °C, respectively. These two temperatures were selected for the following reasons. First, for soldering, the temperature is at least 30–40 °C higher than that of the solder melting temperature. Secondly, the melting temperature of Sn, In, and eutectic In-Sn alloy is 232, 156, and 118 °C respectively. It is clear that the temperature 180 °C is higher than the melting temperature of both In and eutectic In-Sn alloy. As a contrast, the bonding temperature of 150 °C is mere 30 °C higher than the eutectic temperature of In-Sn. Therefore, these two temperatures would help us know how low the temperature can be obtained for wafer-level hermetic bonding using In-Sn solder layers. Dwelling time at the peak temperature was 20 min to ensure sufficient diffusion between solder and high-temperature components. The bonding temperature profile was shown in Fig. 4. After bonding, the bonded wafers were diced into 13 × 13 mm^2 dies with a dicing speed of 2 mm/s.

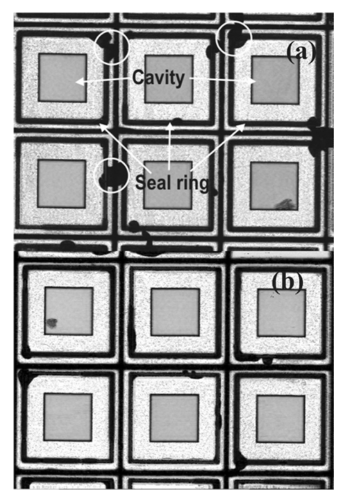

Fig. 5. C-SAM graphs for bonded devices: bonding at (a) 180 °C and (b) 150 °C.

After dicing, all the dies were checked by cross-section scanning acoustic microscopy (C-SAM) for nondestructive study of the bonding interface. The hermeticity of the ring seals for patterned dies was evaluated by helium leak rate tests based on MIL-STD-883. According to the internal cavity volume of the bonded dies ($\sim$0.02 cm^3), the pressure of helium gas in bombing chamber was set as 75 Psi, and exposure time was 2 h. After bombing, the dies were put into helium leak detector to measure the leak rates. For leak rate test, 21 bonded dies were tested.

For microstructure study, five samples for each bonding temperatures were mounted and cross-sectioned for scanning electron microscopy (SEM) observation. These samples were

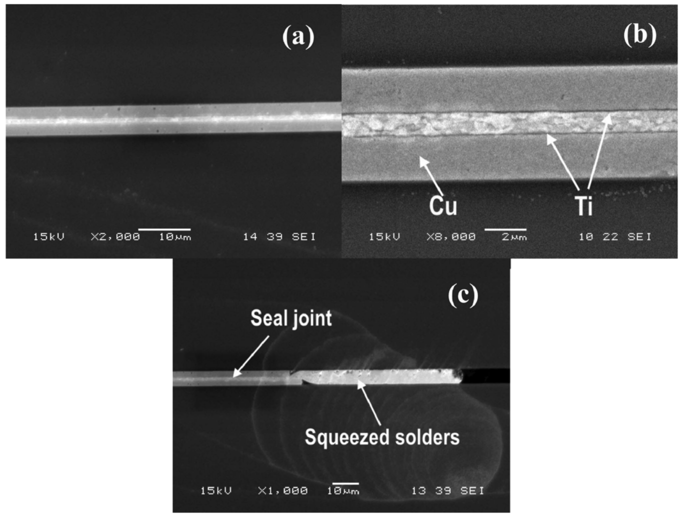

Fig. 6. Interfacial microstructure of seal joint bonded at 180 °C: (a) low magnification, (b) high magnification, and (c) solder squeezed out at the edge of the seal joint.

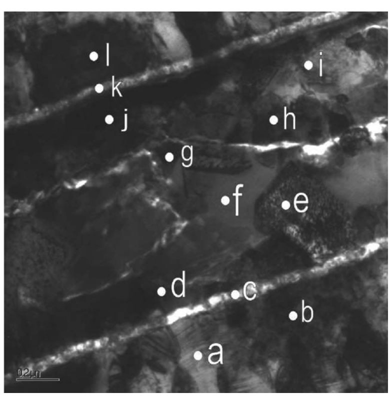

Fig. 7. TEM/EDX analysis for the seal joint bonded at 180 °C.

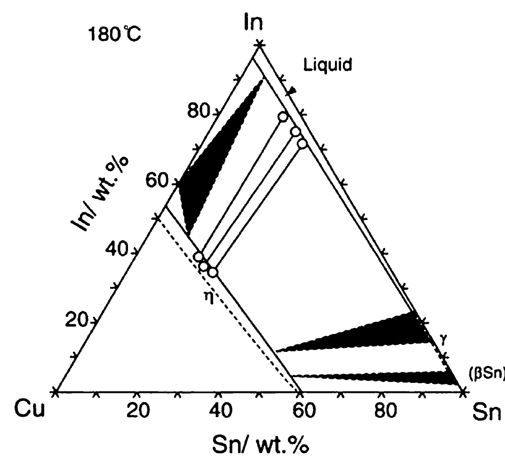

Fig. 8. Isothermal section of Cu-In-Sn system at 180 °C [15].

grinded with SiC paper and polished with 1.0 μm diamond and 0.05 μm silica suspensions. Energy dispersive X-ray (EDX) analysis was used to know the compositions of the bonded ring joints. Focus ion beam was employed to prepare thin film for transmission electron microscopy (TEM) and EDX examination of the joint.

To evaluate the mechanical properties of the seal ring joints, five samples of each bonding conditions were used for shear tests. The shear test was conducted with a shear tester (BT4000 Dage) using a speed of 50 μm/s.

Reliability tests of the boned dies were studied in detail. Pressure cooker test was conducted under 121 °C, 2 atm for 300 h. High humidity storage was done at 85 °C, 85 RH for 1000 hrs. High-temperature storage test at 125 °C and temperature cycling test (−45–125 °C) up to 1000 h were also performed. For each item, 21 samples were tested. After tests, these dies were examined by C-SAM, helium leak rate, and shear tests again. Here, a die with large cracks or with a leak rate smaller than 5×10^{-8} atm · cc/s was considered as a failure sample.

TABLE I
COMPOSITIONS OF SELECTED POSITIONS OF TEM/EDX ANALYSIS

Point	Element (at %)				
	Cu	**Ti**	**Sn**	**In**	**Au**
a	88.1		7.1	4.7	
b	77		11.8	11.2	
c	5.3	79.6	9.9	5.1	
d	12.9	5.7	12.5	47.7	21.2
e	6.8		3	54.8	35.4
f			33.4	18.8	47.8
g	5.7		2.8	60.2	31.3
h	2.4		6.9	59.2	31.5
i	6.1		7.9	54.5	31.4
j	6	4	21.9	44.4	23.7
k	4.8	90.4	2.6	2.2	
l	50.3		30.7	19.1	

III. RESULTS AND DISCUSSION

A. Yield After Dicing and SAM Observation

After dicing, the bonded dies were screened by using C-SAM, and a die was defined as a "good die" if there were no detectable voids and/or cracks. The bonding yield was further defined as

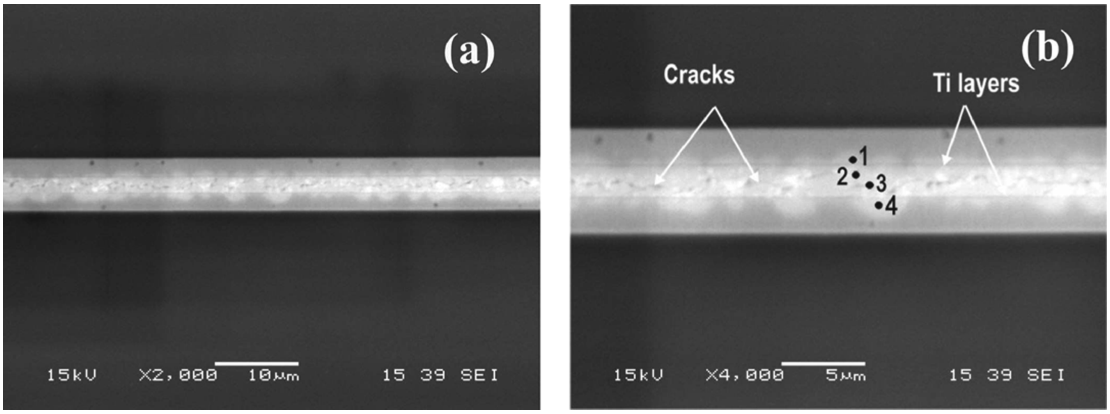

Fig. 9. Interfacial microstructure of seal joint bonded at 150 °C: (a) low magnification and (b) high magnification.

the percentage of good dies to the gross dies of a bonded wafer. After dicing and SAM observation, 100% good seals throughout the 8-in wafer after bonding were obtained both under 180 and 150 °C. As shown in Fig. 5, C-SAM examination revealed good sealing: no voids and holes at the joint. However, it should be pointed out that since the resolution of C-SAM is about several micrometers, small voids cannot be detected. One obvious phenomenon can be found from the C-SAM graphs. Bonding at 180 °C, more solders were squeezed out from the seal joint. As a contrast, when bonding at 150 °C, the solder volume flowing over the seals was quite limited. The reason was very clear: at high bonding temperature, the flowability of liquid solder was better and, under the same pressure, more solders would flow over the seal, especially at the corner regions [marked by circles in Fig. 5(a)]. The maximum distance of the squeezed solder out of the seal was about 2 mm at the corner place. In a tiny package, the flow over of the solders will damage the device inside. The squeezing of solders can be controlled by several methods. One is to reduce the bonding pressure and/or solder thickness but at the same time must ensure the yield. Another method is to make grooves around the seal to prevent the overflow of the solders.

B. *Microstructure of Seal Ring After Bonding*

SEM photos of seal ring joint bonding at 180 °C are shown in Fig. 6. The whole joint after bonding was thinner, and there were no detectable voids and cracks. The thickness of the joint formed at 180 °C was about 5.5 μm where the thickness of IMCs was around 1.5 μm, as shown in Fig. 6(a) and (b). As previously mentioned, a portion of liquid solder was squeezed out during bonding. According to our observation by SEM, normally, the overflow of solder was about 10 μm. As shown in Fig. 6(c), in this graph, the length of the overflowing solder was around $\sim$50 μm at one side of the joint. The composition of the solders was 55–60 at% Sn, 30–35 at% In, and 5–10 at% Au.

TEM/EDX was used to know the accurate compositions along the seal joint. The TEM microstructure is shown in Fig. 7, and the EDX results are listed in Table I. It was quite obvious that two parallel Ti lines were embedded in the joint. According to the EDX results of $\mathbf{c}$ and $\mathbf{k}$,a small amount of In, Cu, and Sn was found in the Ti layer, which meant these elements can diffuse through Ti layer. It proved our proposal to use Ti as the buffer layer for low-temperature wafer-to-wafer bonding. The compositions of $\mathbf{a}, \mathbf{b}, \mathbf{l}$ adjacent to Cu sides proved the above point. For location $\mathbf{a}$ and $\mathbf{b}$, a small amount of Sn and In were found in Cu, which corresponded to the Cu-rich phase. For $\mathbf{l}$, the ratio between Cu and Sn-In is around 1:1. As shown in Fig. 8, according to the thermodynamic calculation of phase equilibrium in a Cu-In-Sn system at 180 °C [15], an η phase existed in the system. It was known that η phase existed in both the two binary systems Cu-In and Cu-Sn, i.e., η-Cu_2In and η-Cu_6Sn_5, with the same NiAs-type structure [16]. According to the study of Sommadossi *et al.* and the high solubility of Sn, the compounds should be η-$Cu_6(Sn\text{-}In)_5$ [16].

TABLE II
COMPOSITIONS AT THE INTERFACE IN FIG. 9(B)

Point	Element (at %)				
	Cu	Ti	Sn	In	Au
1	78.01	5.05	3.48	8.94	4.52
2	60.17	3.31	22.88	13.64	0
3	51.21	2.02	20.86	18.21	7.70
4	72.51	5.49	13.60	8.40	0

For $\mathbf{e}, \mathbf{j}, \mathbf{h}, \mathbf{i}, \mathbf{j}$, the compositions corresponded to $Au(In\text{-}Sn)_2$ phases. The small Cu content may be dissolved in the compounds during liquid/solid diffusion bonding process. For location $\mathbf{d}$, the composition of Cu-Sn-In-Au came from two phases Au-In-Sn and Cu-Sn-In. For point $\mathbf{f}$, the composition fell in Au(Sn-In) phase, which may be formed due to the absence of In atoms since a part of the solder was squeezed out.

SEM photos of seal ring joint bonding at 150 °C are shown in Fig. 9. The thickness of the joint was about 6.5 μm, in which the thickness of IMCs was around 2 μm. Comparing Fig. 6 with Fig. 9, we can also find that the thickness of the joint formed at 150 °C was thicker than that formed at 180 °C. The differences of the two seal joints were mainly caused by the different bonding temperatures. At higher temperature, solder material melted faster and had a better flowability. Under the same pressure, more liquid alloy was squeezed out. So a thin solder joint was formed with a thin IMC layer. Since more solder alloy as kept at 150 °C for diffusion bonding, more solder materials would diffuse through Ti layer into Cu substrates, as shown in Fig. 9(b).

When bonding at 150 °C, due to the low bonding temperature, cracks at the center of seal joint were formed that would be

TABLE III
CHARACTERIZATION RESULTS AFTER RELIABILITY TESTS

Reliability test items	Results	
	Leak rate test (5×10^{-8} atm· cc/sec)	Shear strength (MPa)
Pressure Cooker test	90.5% <5 $\times10^{-8}$	19.88
High humidity	95.2<5 $\times10^{-8}$	17.69
High temperature storage	100% <5 $\times10^{-8}$	15.31
Temperature cycle	90.5% <5 $\times10^{-8}$	18.45
*After bonding	100% <2 $\times10^{-8}$	33.35

harmful to the hermeticity and reliability properties. The reason for the poor bonding qualities is explained in the following. At the surface of the solder materials, after thin Au layer deposition, one thin Au-In layer would be formed. Therefore, in order to form a seal joint, during bonding liquid solders forming both bonding pairs must break through the Au-In layer and meet each other. The melting points of In and Sn are 156 and 232 °C, respectively. Ideally, we hope In-Sn layers can form eutectic alloy with the melting point as low as 118 °C. However, as temperature reached 150 °C, it would take a relatively longer time for In-Sn interdiffusion to form a low-temperature alloy. Even if eutectic alloy was finally obtained, the temperature difference was merely around 30 °C. Under such condition, the flowability of liquid solder and the wetting property were poorer compared with that under high bonding temperature. Therefore, less liquid alloy was pushed through Au-In layers for interdiffusion and joining. As a result, voids along the Au-In layer were formed, and at some place, cracks were generated due to the continuity of the voids.

EDX analysis showed that Sn and In atoms diffused through Ti into Cu and near the Cu regions, Cu_3(Sn-In) phases were formed. At the center region, both $Cu_6(Sn\text{-}In)_5$ and Au-In phases were formed according to the EDX analysis listed in Table II.

C. Hermecitiy and Mechanical Properties of Seal Ring

Helium rate test was performed to examine the hermeticity of the seal. The results showed that the leak rate of the devices bonded at 180 °C was smaller than 2×10^{-8} atm · cc/s, which was smaller than the rejected limit value of MIL-STD-883E, which was 5×10^{-8} atm · cc/s. However, for the devices bonded at 150 °C, only 86% had a leak rate smaller than 5×10^{-8} atm · cc/s.

The average shear strength of the joints formed at 180 °C was 33.35 MPa, and this value for the joints formed at 150 °C was 30.29 MPa. The results indicated robust bonding was obtained. It was surprising that although small cracks were formed when bonding at 150 °C, the joints still maintained high shear strength. It seemed the shear strength was not sensitive to the cracks for this kind of thinner and longer joint composed of high-temperature IMCs.

D. Reliability Properties of Seal Ring

Since the hermeticity of the dies bonding at 150 °C was not very good, for reliability study, only dies bonded at 180 °C were used. The results of reliability tests are listed in Table III. The ratios of dies with a leak rate smaller than 5×10^{-8} atm · cc/s after pressure cooker test, high humidity storage, high-temperature storage, and temperature cycling were 90.5%, 95.2%, 100%, 90.5%, respectively. At the same time, after reliability test, the seal rings can still maintain good mechanical properties. The shear strength after pressure cooker test, high-humidity storage, high-temperature storage, and temperature cycling were 19.88, 17.69, 15.31, and 18.45 MPa, respectively.

The interfacial microstructures after reliability tests were analyzed. As shown in Fig. 10, it seemed there were no changes on the microstructures compared with after bonding. With further SEM/EDX analysis, the compositions of the seal joints also have no detectable changes. The results were reasonable since the temperatures for reliability tests were not very high compared with the melting temperatures of the IMC joints. In addition, the Ti layer can also inhibit the diffusion between Cu and IMCs. However, according to the shear tests, the adhesion between different IMCs decreased after reliability tests.

During long-term reliability tests, we also found diffusion between overflow solder and high-temperature components (Cu, IMCs) had occurred. Fig. 11 shows the microstructure of the sides of the seal joint after high-temperature storage. According to EDX analysis, all the overflowed solders become high-temperature compounds, and tens of micrometer Cu substrates were consumed and turned into $Cu_6(Sn\text{-}In)_5$. For the other three reliability tests, since the test temperatures were not high, the diffusion phenomena were not so extensive. For example, for thermal cycling test, Cu substrates only 10–30 μm in length at each side of the joints were consumed by about 20 μm solders. Because the diffusion has not created new compounds and cracks, it would not cause the failure of seal joints during reliability tests.

Samples with poor hermeticity were also analyzed to know the failure mechanism of the seal joints. Consistent failure mode was confirmed. As shown in Fig. 12, a large crack throughout the seal joint was found. It was clear that the crack expanded along the bonding line between In-Au compounds and Cu-Sn-In compounds. When different IMCs formed at the joints, under thermal cycling and pressure cooker tests, stress would generate. This was the reason why after these two tests, the leak rate test revealed a relative poorer hermeticity results comparing with other tests. It meant that the adhesion between the two phases was the key to determine the reliability of the seal joint. Therefore, two ways can be used to further improve the reliability of the present bonding seal joints. One is to reduce Au-In compounds by thin Au-layer deposition. The other is to reduce the Ti buffer layer thickness to allow fast diffusion between solders and Cu substrate. Then less solder will flow out the joint and thicker IMC joints would be formed with discontinuous Au-In phases.

IV. CONCLUSION

Low-cost and high-yield wafer-to-wafer bonding using an In/Sn solder and a Cu/Ti/Au metallization system was investigated and various tests conducted to evaluate the reliability

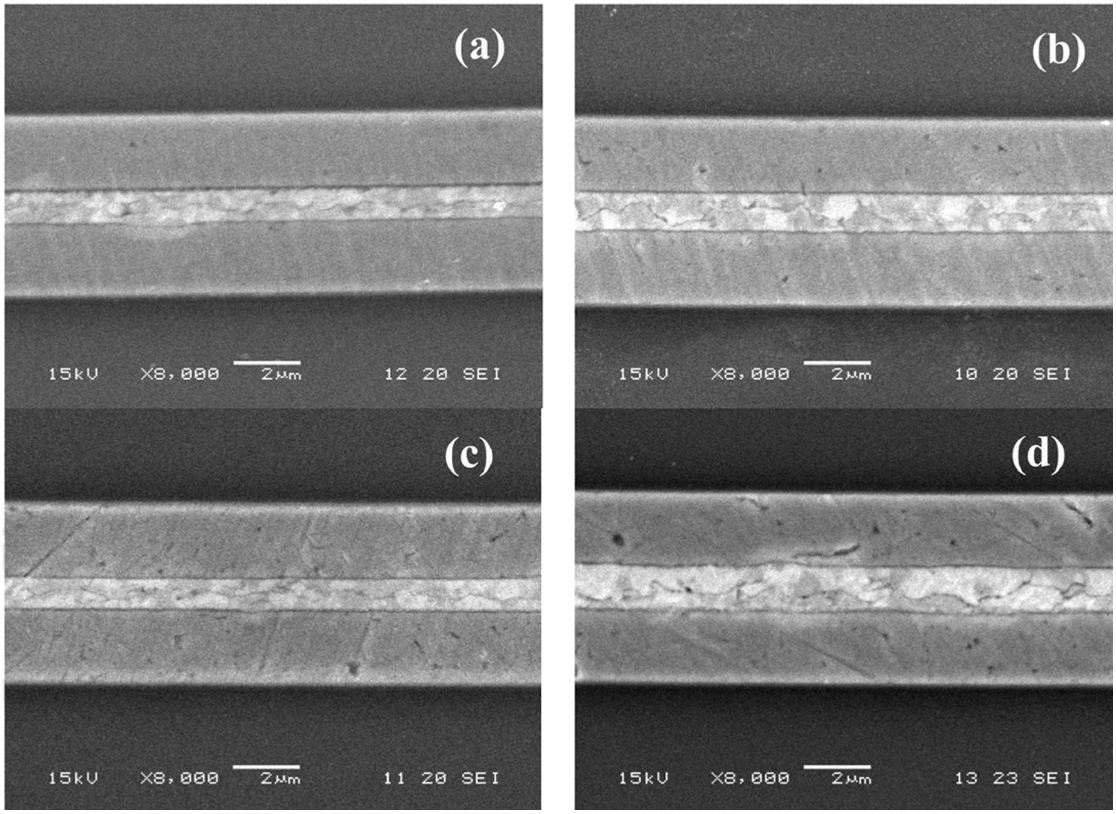

Fig. 10. Interfacial microstructure of seal joint of good dies after reliability tests: (a) pressure cooker test, (b) high humidity storage, (c) high temperature, and (d) temperature cycling.

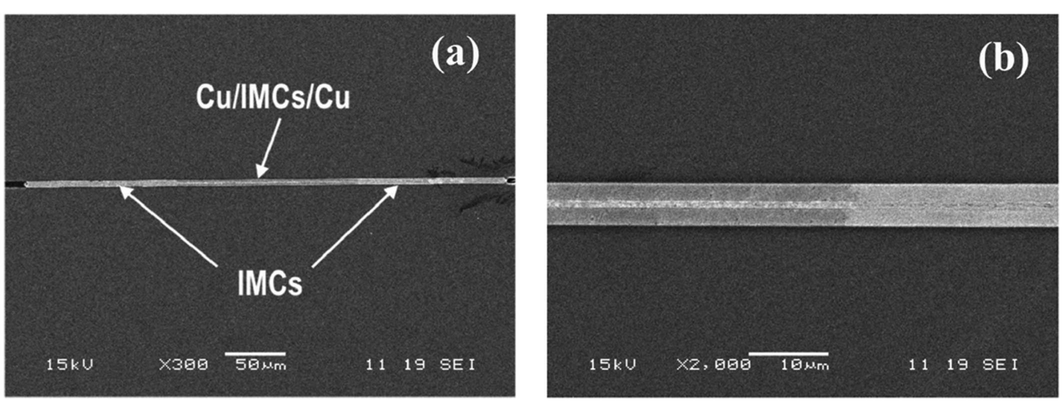

Fig. 11. Diffusion between overflow solder and high-temperature IMC joints after high-temperature storage: (a) low magnification and (b) high magnification.

properties of the bonded devices. Some important results are summarized in the following.

1) No detectable voids were found in the seal rings of all dies after bonding at 150 and 180 °C based on SAM observation.
2) When bonding at 180 °C, all samples obtained good leak rate ($< 2 \times 10^{-8}$ atm · cc/s). While bonding at 150 °C, 86% of dies can get acceptable hermeticity. The sample size in both cases is 21.
3) Under the two bonding temperatures (150 and 180 °C), In and Sn atoms can diffuse through Ti layer to form joint with Cu. Seal joints were composed of high-melting-point IMCs, which allow the dies for next level higher temperature interconnections. It was found that more solders would be squeezed out when bonding at 180 °C.
4) Under bonding at lower temperature, e.g., 150 °C, a thick seal joint was obtained due to the low flowability of liquid alloy. However, cracks were formed at the center of the seal rings, which caused the hermeticity problem.
5) After bonding, high shear strength was obtained for the seal rings formed under both bonding temperatures (150 and 180 °C).
6) After four kinds of reliability tests—pressure cooker test (121 °C, 2 atm, 300 h), high-humidity storage (85 °C, 85 RH, 1000 h), high-temperature storage (125 °C, 1000 h), and temperature cycling test (−45–125 °C, 1000 h)—dies

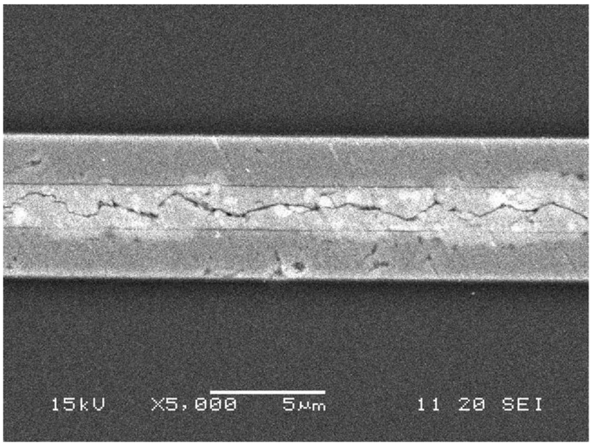

Fig. 12. Interfacial microstructure of the failed seal joint after pressure cooker test.

bonded at 180 °C showed good reliability properties by hermeticity and shear tests.

7) The propagation of a crack along different IMC layers was found in the failed dies after reliability tests. Therefore, the adhesion between different phases was the key to determining the reliability of the seal joint. During long-term reliability tests, diffusion between overflow solder and high-temperature components (Cu, IMCs) had occurred.
8) These results indicate the current material system (Cu/Ti/Au) with the bonding parameters (180 °C for 20 min under 5.5 MPa) can be used for MEMS packaging applications, which require low-temperature hermetic sealing.

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