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Characterization of intermediate In/Ag layers of low temperature fluxless solder based wafer bonding for MEMS packaging

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ABSTRACT

Low temperature fluxless solder for wafer bonding has received a lot of attention due to its great potential in hermetic MEMS packaging. Previous research activities mainly deploy solder alloy of eutectic composition to achieve low bonding temperature. We proposed new intermediate bonding layers (IBLs) of rich Ag composition in In–Ag materials systems. In this study, we investigated the intermetallic compounds (IMCs) at the bonding interface with respect to the bonding condition, post-bonding room temperature storage and post-bonding heat treatment. With this IBL, the IMCs of Ag_2In and Ag_9In_4 with high temperature resist to post-bonding process are derived under process condition of wafer bonding at 180 °C, 40 min and subsequent 120–130 °C annealing for 24 h. Low melting temperature IMC phase of $AgIn_2$ is formed in the interface after long term room temperature storage or 70 °C aging treatment. This low melting temperature IMC phase can be completely converted into high melting temperature IMCs of Ag_2In and Ag_9In_4 after 120 °C additional annealing. Based on our results, we can design the packaging process flow so as to get reliable hermetic packaged MEMS devices by using low temperature fluxless In–Ag wafer bonding.

1. Introduction

Transducer mechanisms, structures, materials and fabrication technologies for microelectromechanical system (MEMS) devices change depending upon their applications. The MEMS packaging technologies remain as application-specific solutions [1,2]. Thus the packaging of MEMS devices is considered as the most challenge tasks of MEMS commercialization. The MEMS packaging technology typically is categorized as two groups in terms of wafer scale and chip scale. The main consideration is that the free-standing and fragile MEMS structures either have to be protected properly before the chip singulation step, e.g. saw dicing, or must be strong enough for withstanding saw dicing step. General speaking, suitable technologies for MEMS packages typically need to provide sealing or encapsulation of MEMS structures, electrical feedthroughs and pathways of that MEMS devices can interact with ambient so as to either sense the change or introduce a change. Wafer scale packaging is considered as the lower cost approach than chip scale solution typically because it may offer sealing and electrical feedthroughs via wafer bonding step. Thus various wafer bonding technologies have been investigated for MEMS packaging applications. These wafer bonding technologies are categorized as two approaches, i.e., direct bonding and in-direct bonding, i.e., the intermediate layer bonding. The direct bonding approach include technologies such as, silicon fusion bonding at about 1000 °C [3], Si/glass anodic bonding at about 450 °C [4], plasma surface activated bonding at 450 °C in vacuum [5] and even at room temperature in vacuum [6] and in ultrahigh vacuum [7]. On the other hand, the choice of the intermediate bonding layer (IBL) will be made according to the type of substrates to be bonded and whether there is a requirement of hermetic sealing or not. The well-known intermediate layer bonding are polymer based bonding at temperature ranging from 100 °C to 150 °C [8,9], Au/Sn solder based eutectic bonding at 280 °C [10,11], Au/Si eutectic bonding at 365 °C [12], and glass frit bonding at 400 °C [13,14]. In view of most of applications that need to have the hermetical sealed packages, polymer based intermediate layer bonding has gas permeable interface and does not meet the hermetic sealing requirement. Therefore, Au/Sn solder bonding

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and glass frit bonding are the main stream approaches in MEMS industry nowadays.

Besides a lot of MEMS devices contain different materials or need to bond substrates containing the electronic part of the devices (e.g. CMOS wafers). Thus the difference in thermal expansion coefficients of the dissimilar materials results in a mechanical stress in proportion to process temperature. It points out that low temperature wafer bonding technology is a key for avoiding such residual mechanical stress due to aforementioned reasons.

To fulfill the hermetic sealing and low process temperature, Indium and indium-based alloy solders have been reported to be very attractive intermediate layer materials. Since the In–Sn material system has eutectic point at 118 °C and pure indium is melted at 156.6 °C. Several literatures have reported the chip-to-chip low temperature bonding by using In–Sn, In–Ag, In–Cu and In–Au [15–20], while the wafer level packaging using In–Sn eutectic solder bonding [21] and In compression bonding [22–24] have been reported. Moreover, industry also requires that the formed solder-bonded interfaces can be survived at temperature at least as high as 285 °C which is the peak temperature in the surface mounting technology (SMT) manufacturing line. It means that the resulted intermetallic compounds (IMCs) of the solder-bonded interfaces in any post-bonding steps need to have melting temperature, i.e., defined as re-melting temperature, higher than the post-bonding process temperature. In this paper, we are working on In–Ag low temperature solder based wafer bonding with aim of materials evolution of the resulted IMCs at the bonded interfaces with respect to various post-bonding heat treatment process condition.

2. Intermediate bonding layer design and experimental condition

As we described in introduction, it is very intriguing to develop reliable metallurgy using In–Ag materials system for wafer level MEMS packaging. In the In–Ag phase diagram (Fig. 1) [25], the eutectic temperature is observed as 144 °C at 96.5 wt.% In, while the melting temperature of indium and silver is referred to 156.7 °C and 961.9 °C, respectively. Chuang and Lee have reported that In–Ag chip-to-chip is successfully bonded at temperature slightly above 200 °C and with additional 150 °C annealing in hydrogen environment [17]. The derived bonding interface shows high re-melting temperature. It points out that the resulted bonding interface was produced by consumption of all the indium in the bonded couple to form Ag_2In IMC phase.

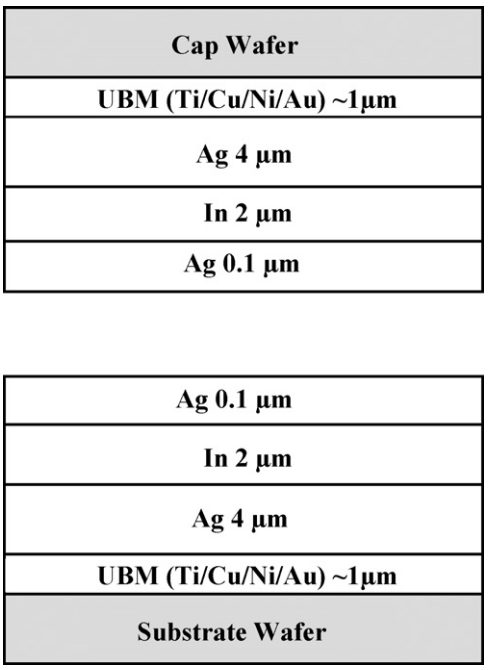

Fig. 2. The intermediate bonding layers on both sides of bonding pair wafers, where the schematic drawing showing thin silver coated surface of both sides are face to face arranged.

More clearly speaking, reliable bonding can be realized by a flux-less soldering approach that comprises IBL combinations including a low melting point (LMP) component, e.g. In or Sn, and a high melting point (HMP) component, e.g. Au, Ag, or Cu. Without using the eutectic composition, e.g. 96.5 wt.% In of In–Ag system, the HMP/LMP ratio of overall IBL is selected to be higher enough. Therefore the LMP component is essentially depleted into HMP layer and reacted into an IMC that has a higher melting temperature, i.e., the re-melting temperature, than the original melting temperature of LMP component. Thus, as shown in Fig. 2, we propose an IBL com-

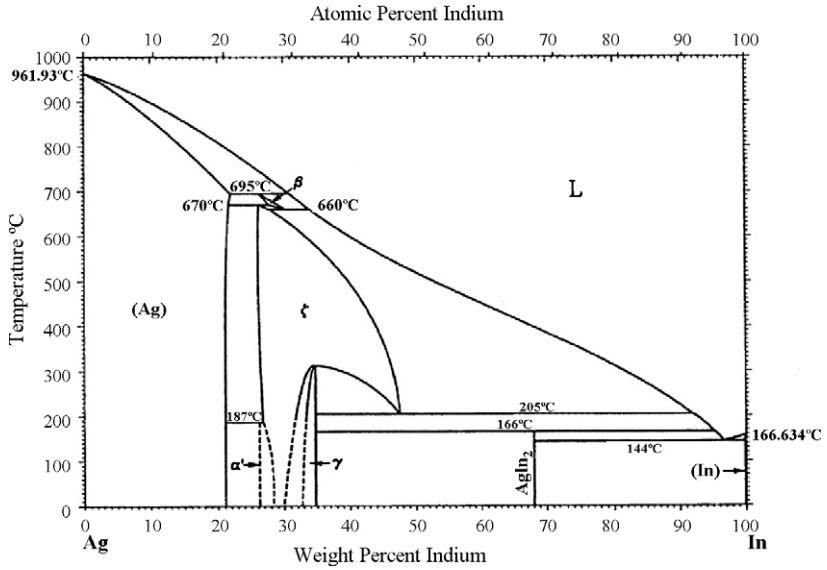

Fig. 1. The In–Ag phase diagram.

bination which was prepared on both bonding-surfaces of a pair of wafers. The IBLs include 2 μm In and 4 μm Ag layers, in which they are evaporated and patterned by using lift-off process on top of Si device wafer coated with Ti 300 Å/Cu 3000 Å/Ni 5000 Å/Au 1000 Å under bump metallization (UBM) layer. Due to high interdiffusion rate within layers of IBL, some sorts of IMCs can be formed between the noble metals and indium even at room temperature. We take this advantage and prepare a thin Ag layer of 1000 Å on top of In layer so as to form the $AgIn_2$ thin layer at the surface. It can prevent the oxidation of underneath In layer, when these wafers are prepared and exposed to air after chamber opening. We can avoid the flux treatment on wafer surface before wafer bonding step. So we say it is a fluxless process. The weight percentage of 2 μm In layer versus 4 μm Ag layer is 25.4%. From Fig. 1, this 25.4 wt.% In composition implies that the homogeneous phase of the bonded interface layer will be the solid solution of α′ phase and Ag. But the actual IMC phases of the bonded interface layer is strongly depending on the layer sequence, interdiffusion process and bonding condition. In addition to the α′ phase, more IMC phases with In of 22 wt.% up to 34 wt.% are expected to be observed from our experimental results. Practically the IMC phases containing In within this weight percentage range are the γ, ζ and β, where these are the stable phases in each specific temperature range from ambient up to 695 °C. Again, from Fig. 1, we should notice that the melting point of IMCs increases with the silver content, i.e. eutectic composition (144 °C) < $AgIn_2$ (166 °C) < γ (300 °C) < ζ (670 °C) < β (695 °C) [26].

In order to explore the feasibility of the MEMS packages based on this concept, we develop an integrated process flow for making micromirror wafer and cap wafer. The wafer used for constructing micromirror is a silicon-on-insulator (SOI) wafer. Thicknesses of device layer, buried oxide (BOx) layer and handle wafer are 30 μm, 2 μm and 690 μm, respectively. Two steps of inductively coupled plasma (ICP) deep reactive ion etching (DRIE) process are carried out to fabricate the comb actuator structure and to open the backside cavity of the whole device, respectively. Fig. 3(a) and (b) shows the schematic drawing and SEM photo of a micromirror device, respectively. The center white area represents the reflection mirror. A Pyrex glass wafer (Corning 7740) is bonded to the backside of the micromirror wafer in order to seal the backside opening. The anodic bonding is carried out in at 400 °C and 450 V. After the mirror wafer is bonded on this glass wafer, a dry film of photo resist is attached and lithographed on top of mirror wafer. The In/Ag IBL is prepared by evaporation and lift-off steps. Finally the whole mirror device is enclosed by an In/Ag IBL ring.

Moreover, a cap wafer containing a Pyrex glass wafer (Corning 7740) and the same In/Ag IBL ring is prepared separately. During bonding process, these wafers are aligned and put into bonding chamber of 6 mTorr first. Then the fluxless solder bonding is conducted at 180 °C for 40 min under 8 kN of applied bonding force. The bonding force is about the highest force that we can apply due to bonding equipment set up. The bonding temperature of 180 °C and time of 40 min are selected according to our previous chip-to-chip bonding results based on Ag rich IBL design [27]. More specifically, we have used X-ray diffraction (XRD) method to identify the crystalline phases of bonded interface by looking into the surface of separated chips which were successfully bonded at 180 °C. Clear Ag_2In and Ag_9In_4 IMC phases are observed for the cases with different bonding time [27]. Both of hermetical sealed ring and electrical interconnects are formed at this bonding step. As shown in Fig. 3(a), two metal posts on mirror chip are electrically separated by the silicon trench. These two metal posts are electrically connected via a metal line on cap glass wafer side. This metal is cross underneath solder sealing ring with dielectric layer passivation. Thus the hermetic sealing can be kept inside the sealed cavity.

Fig. 4 (a) is the photo of the top view of bonded 8″ wafers. Photo of wafer bonding packaged micromirror chip after dicing is shown in Fig. 4(b), while Fig. 4 (c) shows the X-ray image of the bonded wafer in which it is taken from the cap wafer side. The bright square shown in the center of micromirror chip of Fig. 4 (b) is the reflective micromirror. Then the wafer bonding packaged micromirror chip is assembled on a dual-in-line package (DIP) carrier for further device function test, as shown in Fig. 4 (d). We have reported design and features of the micromirror elsewhere [28]. The micromirror is actuated by the electrostatic force vertical comb fingers under pulse wave bias. The operation scheme of this kind of micromirror can be found in reference [29,30]. In this paper, we focus on the investigation of IMC formation mechanism and materials evolution of the bonded interface with respect to post-bonding heat treatment and storage conditions.

3. Results and discussions

3.1. Effect of post-bonding annealing

First of all, we conducted the post-bonding annealing at 130 °C for 24 h for the wafer bonding packaged mirror chips after dicing in N_2 filled furnace. Properly diced chips were mounted on epoxy resin and subsequently polished. Cross section elemental composition of bonded interface was characterized by energy dispersive X-ray spectroscopy (EDX). Samples were mounted on epoxy resin and subsequently polished. Fig. 5 shows the weight percentage of all the components as a function of the depths along the bonded interface. Along the cross section of the bonded interface, it is observed that

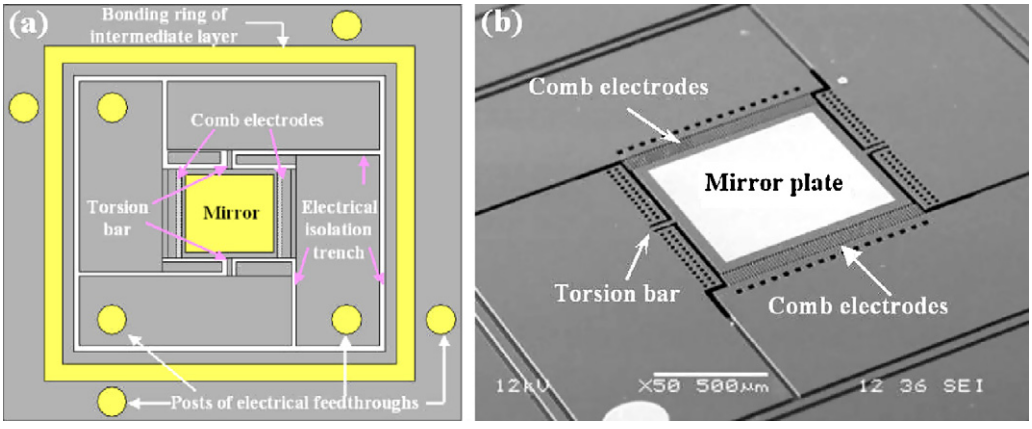

Fig. 3. The schematic top view drawing of micromirror device (a); the SEM photo of fabricated micromirror with two sets of vertical comb electrodes and torsion bar (b).

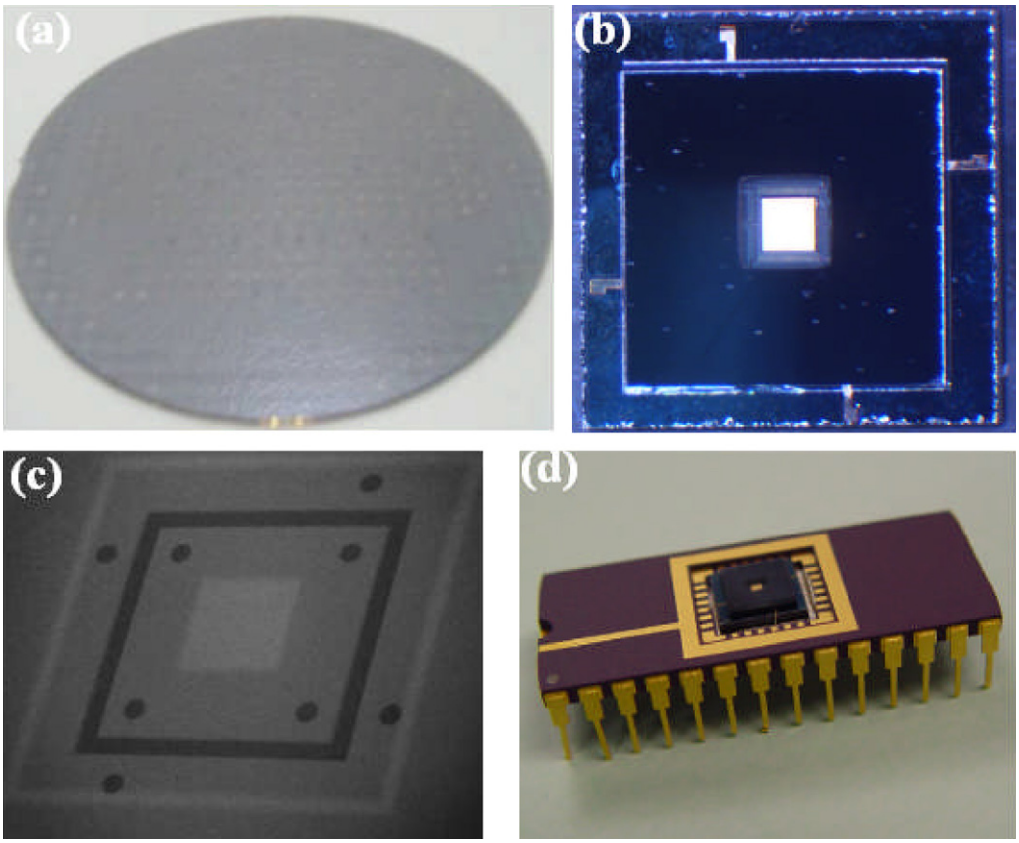

Fig. 4. The bonded stack-wafers with 8″ diameters (a); top view photo of separated micromirror chip with the reflective mirror at the center (b); X-ray image of one chip area of cap wafer with bonding ring shown in dark square ring pattern (c); photo of diced micromirror chip after assembled on DIP carrier (d).

there is an intermediate layer of a homogeneous composition with thickness about 7.5 μm at the center zone. The composition ratio of this intermediate layer is referred to Ag_9In_4 IMC phase mainly, while the IMC phase at the position of 7 μm is suggested as Ag_2In phase. Since both Ag_2In and Ag_9In_4 are the observed phase according to the crystal structure analysis by XRD data for the samples bonded at 180 °C [27]. It is also noticed that there is a thin pure Ag layer of about 1 μm thickness shown on both sides of IBL. These two pure Ag layers can be referred to the remaining Ag on top of UBM layers on two bonding pair wafers. It also means that the current IBL design leads to IMCs of high re-melting temperature, e.g. γ of 300 °C and ζ of 670 °C. In other words, the HMP/LMP ratio of IBL in Fig. 2 is an appropriate combination. The bonded interface of Ag_9In_4 and/or Ag_2In IMC phases and pure Ag will promise the derived MEMS package with good high temperature resistant characteristics against to post-bonding process temperature, e.g. SMT peak temperature of 285 °C.

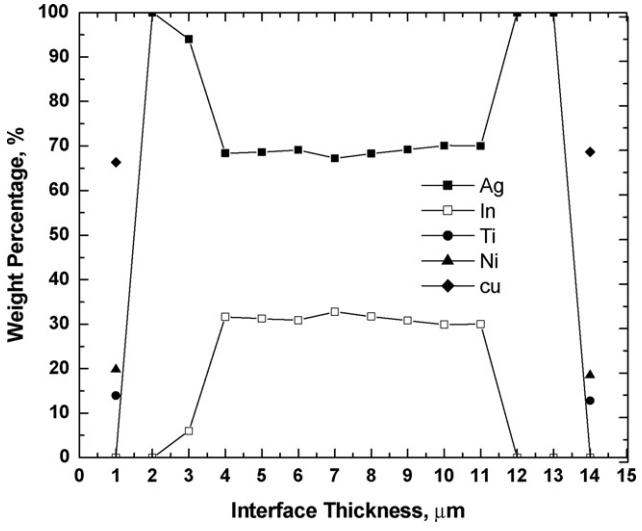

Fig. 5. The EDX analysis data along the cross section of bonded interface.

3.2. Effect of long term room temperature storage

It has been reported that Ag_2In and $AgIn_2$ are the stable phases at temperature above and below 100 °C in an In–Ag diffusion couple experiment using thick foils of pure In and Ag [29]. When the diffusion couple with dominant IMC of Ag_2In cooled down and maintained at room temperature for a long time, Ag atoms diffused from some Ag_2In grains into adjacent pure Ag grains, and In atoms from adjacent pure In grains diffused into these Ag_2In grains. Some of these Ag_2In grains gradually became $AgIn_2$ grains. In a later stage, the grain boundary of these $AgIn_2$ grains continuously expend by consuming adjacent Ag_2In grains, i.e., the grain growth process. Eventually $AgIn_2$ became the major IMC phase along the interface of diffusion couple after room temperature storage for a long time, e.g. 1 month [31]. According to this information, we have kept diced chips in N_2 filled container at room temperature for 80 days, where these chips were derived from bonded wafers which were bonded at 180 °C for 40 min. We investigated the bonded interface of these chips in terms of EDX analysis. Fig. 6(a) shows the SEM photo denoted with the phase composition along the bond-

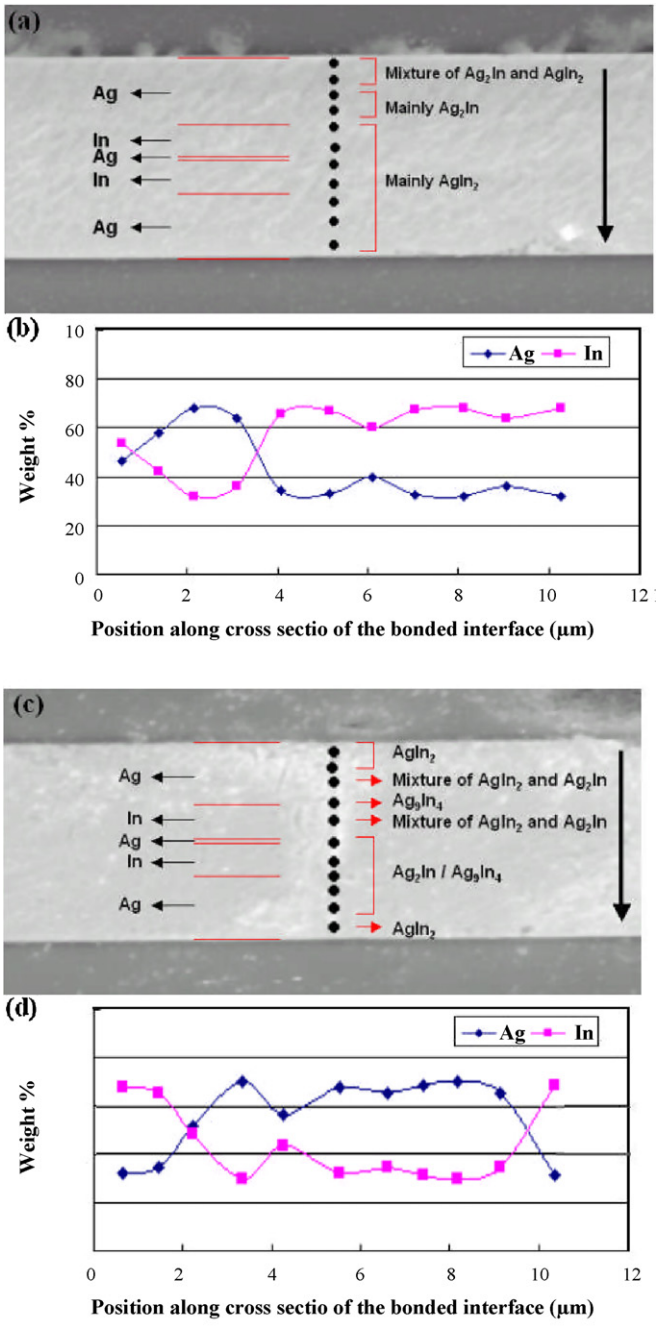

Fig. 6. Study of bonded interface under long term room temperature storage effect: (a) SEM photo denoted with identified IMC phases of first chip; (b) the EDX data derived from spots shown on (a); (c) SEM photo denoted with identified IMC phases of second chip; (d) the EDX data derived from spots shown on (c).

ing interface cross section, while the Fig. 6(b) are the measured EDX results which is plotted versus the position of bonding interface. Besides, the original positions of all layers except the UBM are marked on the left side of Fig. 6(a) as well. Fig. 6(c) and (d) is the results derived from another chip. First of all, no pure In phase is observed. We also conclude that both Ag_2In and $AgIn_2$ coexist in the bonding interface after room temperature storage of 80 days. Some data points are derived with weight percentage close to Ag_9In_4, as shown in Fig. 6(c). For example, the composition at 3.3 μm of Fig. 6(d) is matched with Ag_9In_4. This observation is in agreement with previous bulk-based diffusion couple results [29].

3.3. Effect of Aging

When we consider the post-dicing chip assembly process, such process typically involves with baking of solvent and/or curing at low temperature. Besides, in the case that the packaged MEMS devices used in some high temperature environment, what is the influence of such aging treatment. Thus we have kept diced chips in N_2 filled container at 70 °C for 80 h, where these chips have been stored at room temperature for 80 days and were derived from a bonded wafer which was bonded at 180 °C for 40 min. The EDX results of the cross section of the bonded interface are shown in Fig. 7(a)–(c). We have conducted several line scan analysis. Two of these line scan data are plotted in Fig. 7(b) and (c). These data consistently show that amount of $AgIn_2$ phase is increasing when we compares these samples with room temperature long term storage samples and the as-bonded samples too. Besides, the bonding interface does not convert into single IMC phase of $AgIn_2$ in after this 70 °C for 80 h aging. Due to that the original weight ratio of Ag/In of present IBL combination is 2.94, we strongly believe that the single IMC phase of $AgIn_2$ will never happen at the bonding interface even after extremely long time of low temperature aging. However, the melting temperature of $AgIn_2$ is 166 °C. Thus the existing $AgIn_2$ may be a concern regarding to long term reliability.

3.4. Effect of additional annealing

In the last part of experiment, we explored the influence of annealing. We have kept diced chips in N_2 filled container at 120 °C for 80 h, where these chips have been stored at room temperature for 80 days and were derived from a bonded wafer which was

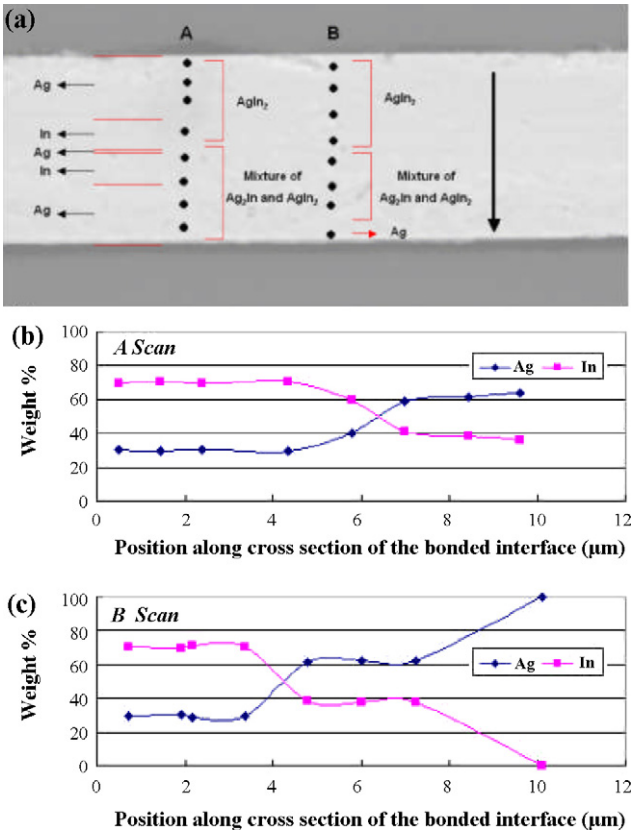

Fig. 7. Study of bonded interface under low temperature aging effect: (a) SEM photo denoted with identified IMC phases; (b) the EDX data derived from A scan line shown on (a); (c) the EDX data derived from B scan line shown on (a).

bonded at 180 °C for 40 min. The SEM photo and line scan based EDX results of the cross section of the bonded interface are shown in Fig. 8(a)–(c), respectively. Interestingly single phase IMC of Ag_2In has been observed and occupies the major portion of bonding interface. Comparing with the case in Fig. 5, i.e., with existing pure Ag phase at both sides, Fig. 8 shows very limited thickness of remaining phase other than Ag_2In. This result points out that appropriate low temperature annealing, e.g. at 120 °C for 80 h, can effectively get rid of low melting temperature IMC phase, i.e., $AgIn_2$. In particular, the composition at 2 μm position of a scan in Fig. 8(a) is quite close to Ag_9In_4. We can image that such annealing of 120 °C for 80 h could be well accepted by most packaged MEMS devices. So we can apply this annealing step to refine the microstructure of sealing rings of packaged MEMS devices.

On the other hand, some micro-cracks are observed at the bonding interface for the samples underwent even longer time of annealing step, i.e., 120 h at 120 °C. Fig. 9 shows that the dominant phase are Ag_2In and Ag_9In_4, while micro-crack appears at the bonded interface. Both Ag_2In and Ag_9In_4 are the high melting temperature phases and are desired to be the final IMCs at the interface. Moreover, in order to explore the facts responsible for such micro-cracks, we calculate the density of $AgIn_2$ as 8.43 g/cm^3 and the density of Ag_2In, as 9.78 g/cm^3 first. Then we derive that the corresponding volume change of $AgIn_2$ in unit mass to Ag_2In in unit mass is an increment of 13.8%. The IBL ring structure is confined between two substrates and cannot absorb such 13.8% volume expansion easily. Thus the residual stress leads to the observed micro-cracks eventually. The meander trace of IBL ring and narrow ring may be possible ways of releasing the residual stress so as to avoid the micro-crack generation.

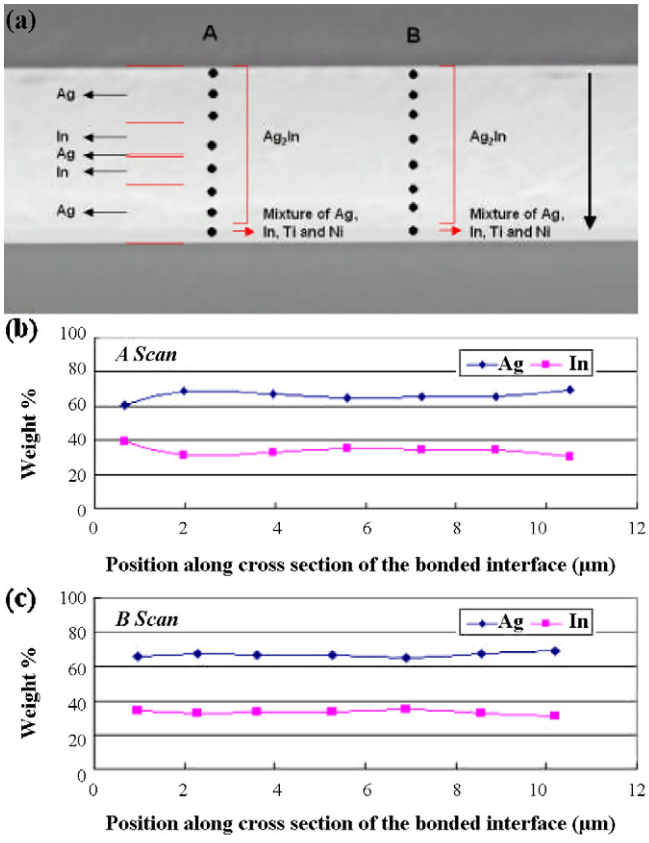

Fig. 8. Study of bonded interface under additional annealing effect: (a) SEM photo denoted with identified IMC phases; (b) the EDX data derived from A scan line shown on (a); (c) the EDX data derived from B scan line shown on (a).

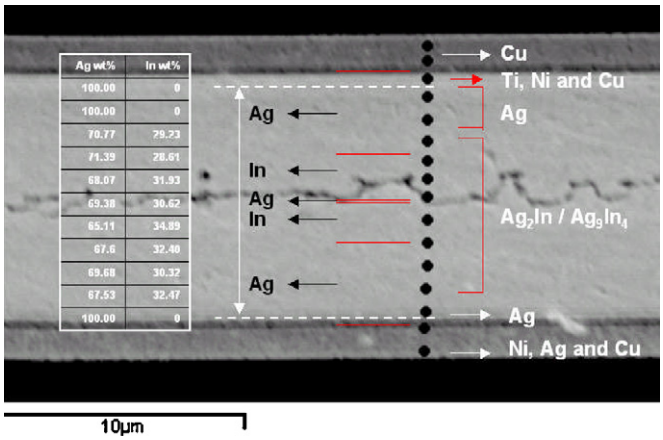

Fig. 9. SEM photo of bonded interface after prolonged additional annealing where the EDX results are denoted on left side and suggested IMC phases are depicted on right side.

4. Conclusions

It is the first time that the feasibility of wafer bonding based MEMS packaging using In/Ag non-eutectic solder as the IBL has been reported. The concept of high ratio of HMP/LMP is successfully implemented in formation of IMCs with high temperature resistant characteristics in post-bonding process. Wafer level packaging deploying wafer bonding at 180 °C, 40 min and subsequent 120–130 °C annealing for 24 h can produce single IMC phase of Ag_2In at the interface. IMCs of coexisted Ag_2In and $AgIn_2$ have been identified at the interface of bonded samples when these samples have been stored at room temperature for months. Aging treatment of 70 °C, 80 h for those samples after long term room temperature storage can increase the relative amount of $AgIn_2$ in IMCs at the interface. However, the bonded interface will never become single IMC phase of $AgIn_2$ because the initial IBL with 25.4 wt.% In only.

High melting temperature IMCs of Ag_9In_4 and Ag_2In at the interface are derived after additional annealing of 120 °C, 80 h for those samples after long term room temperature storage. The melting temperature of IMCs of Ag_9In_4 and Ag_2In is higher than 400 °C [27]. It implies that appropriate annealing can get rid of low melting temperature IMC phase, i.e., $AgIn_2$. However the prolonged annealing in this situation leads to generation of micro-cracks due to IBL ring facing significant volume change from phase transformation, i.e., from $AgIn_2$ into Ag_2In.

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