

# Design and optimization of wafer bonding packaged microelectromechanical systems thermoelectric power generators with heat dissipation path

Chengkuo Lee<sup>a)</sup>

Department of Electrical and Computer Engineering, National University of Singapore,  
4 Engineering Drive 3, Singapore 117576, Singapore and Institute of Microelectronics (IME),  
Agency for Science, Technology and Research (A\*STAR), 11 Science Park Road, Singapore Science Park II,  
Singapore 117685, Singapore

Jin Xie

Institute of Microelectronics (IME), Agency for Science, Technology and Research (A\*STAR),  
11 Science Park Road, Singapore Science Park II, Singapore 117685, Singapore

(Received 12 September 2008; accepted 3 November 2008; published 26 May 2009)

A new concept of microelectromechanical system based thermoelectric power generator (TPG) with unique heat dissipation path is investigated in this study. By using solder based wafer bonding technology, the authors can bond three pieces of wafers to form vacuum packaged TPG. According to the finite element method and analytical modeling results, the output power per area of device is derived as  $68.6 \mu\text{W}/\text{cm}^2$  for temperature difference of about  $6^\circ\text{C}$  between two ends of thermocouple junctions. It shows that the proposed device concept is an effective and low cost approach to enhance the output voltage. © 2009 American Vacuum Society.

[DOI: 10.1116/1.3046155]

## I. INTRODUCTION

Traditionally, electronic devices have relied on batteries as the power sources because they are reliable, easily accessible, and convenient to use. However, batteries can only operate over a finite period of time, after which they will have to be changed. Frequent replacement of batteries is not appropriate in few applications such as implantable biomedical devices and wireless sensor networks in harsh environment. Clean energy such as solar energy and microelectromechanical system (MEMS) energy harvesters are promising alternatives. Silicon solar cell of average efficiency can produce about  $15 \text{ mW}/\text{cm}^2$  under direct sunlight, while the same solar cell can only produce about  $10 \mu\text{W}/\text{cm}^2$  in normal office lighting. Advances in low power very large scale integrated design and complementary metal oxide semiconductor (CMOS) fabrication have reduced power requirements for integrated circuits to the point that self-powered wireless sensor network nodes are now feasible. Vibration based MEMS energy harvesters have been investigated for power sources of wireless sensor network applications.<sup>1,2</sup> MEMS energy harvesters using thermoelectric energy transduction mechanism are a promising power source in the realization of a body area network which consists of a set of wireless sensors and actuators for providing health, sports, comfort, and safety monitoring functions to the users.<sup>3</sup> The thermoelectric method can convert ambient heat flux (thermal energy) into voltage output (electrical energy). In other words, thermoelectric devices convert waste heat from human body into electrical power, i.e., the thermoelectric power generators (TPGs). The *n*-doped and *p*-doped polycrystalline silicon are the available thermoelectric materials

in CMOS process.<sup>4</sup> With the aids of MEMS technology, we can make very thin membrane structure comprising *n/p* poly-Si thermocouples by deploying the bulk micromachining to remove the underneath silicon substrate.<sup>5,6</sup> The appropriate heat flux path is necessary to be managed in order to create the largest temperature difference between two ends of thermocouples, i.e., the hot and cold junctions. The output voltage of TPGs is in proportion to said temperature difference. We proposed a new MEMS TPG configuration in wafer bonding packaged vacuum structure. We introduced a new concept of heat dissipation path (HDP) for enhancing the temperature difference between hot and cold junctions. The focus of this article is to develop an approach of design and optimization of this vacuum packaged MEMS TPGs.

## II. DEVICE CONFIGURATION AND DESIGN CONSIDERATION

Recently a membrane-type MEMS TPG with underneath air cavity encapsulated by wafer bonding process has been reported by Huesgen *et al.*<sup>7</sup> Besides, the SU-8, a polymer with high thermal resistance has been deposited on the top surface of TPG to block the heat loss and to confine the thermocouples as the main heat path, while an additional overcoat of gold film on SU-8 is made to guiding the heat flowing toward the main heat path. We propose a new MEMS TPG design to improve the output voltage by using solder based wafer bonding technology<sup>8-10</sup> to form sealed vacuum cavities on both sides of MEMS TPG. As shown in Fig. 1, a bottom silicon wafer is bonded to MEMS TPG wafer with back side opening in vacuum chamber. Thus the underneath cavity is sealed in vacuum. A cap wafer with cavities is further bonded to the top surface of MEMS TPG wafer such that a top vacuum cavity is formed. To illustrate our concept, the cross-section views of proposed MEMS

<sup>a)</sup>Author to whom correspondence should be addressed; electronic addresses: elelc@nus.edu.sg and leec@ime.a-star.edu.sg

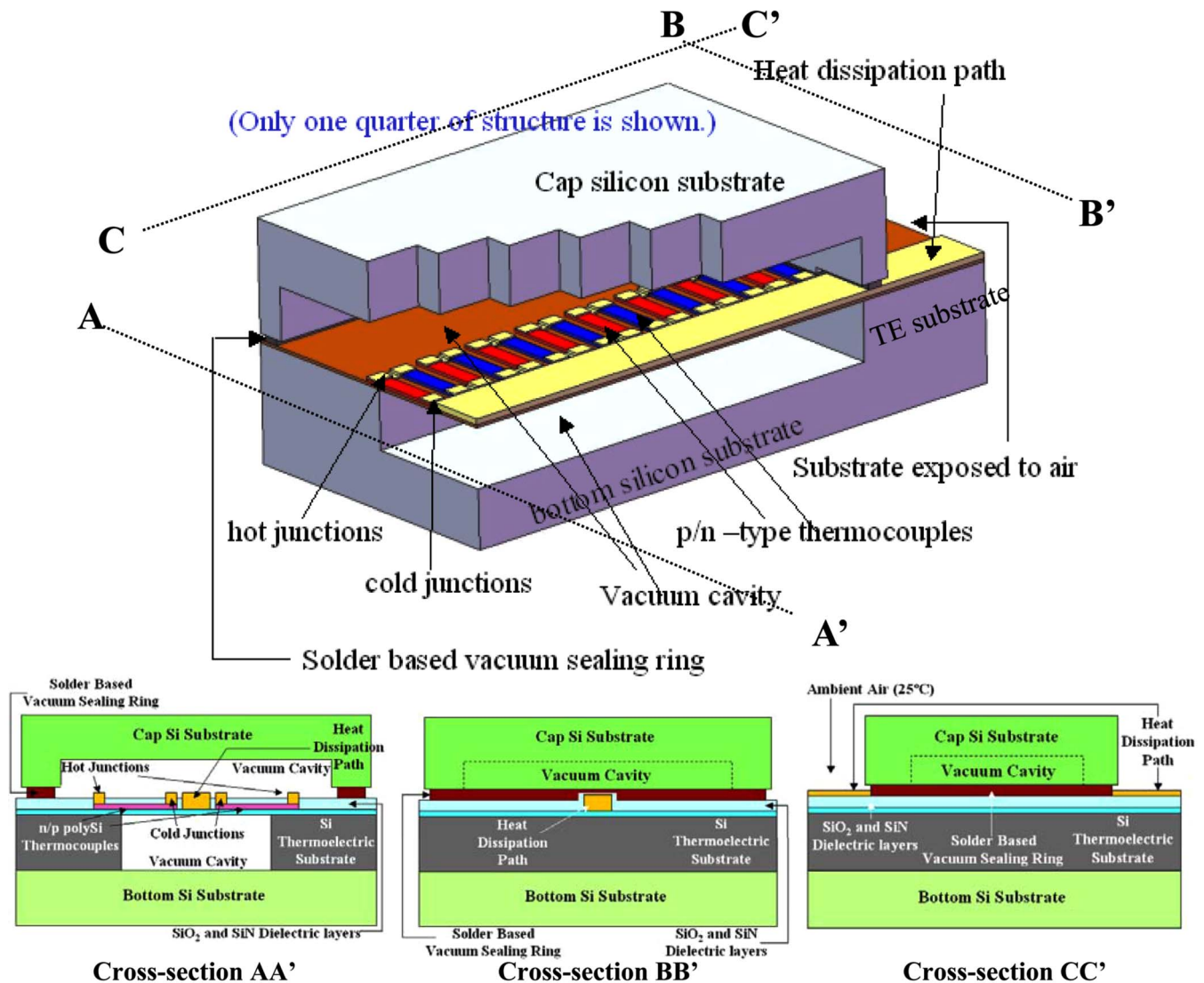


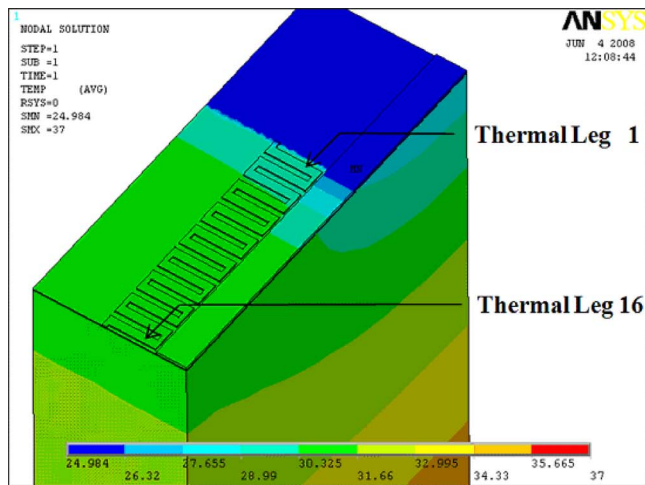
FIG. 1. (Color online) Schematic of the MEMS TPG with two vacuum cavities formed by wafer bonding (only one quarter of structure is shown), where the TPG view along thermocouple strips ( $A-A'$  line) is shown in left bottom; the TPG view along the edge of chip ( $B-B'$  line) is shown in middle bottom; the right-bottom drawing is the TPG view along longitudinal direction of heat dissipation path ( $C-C'$  line) when we look at the sidewall of three bonded chips.

TPG along  $A-A'$ ,  $B-B'$ , and  $C-C'$  lines have been depicted in bottom insets of Fig. 1. The bottom side of Si substrate can be attached on the human skin or any other hot objects available, while the peripheral surface of Si thermoelectric substrate is exposed to ambient air of  $25^\circ\text{C}$ , as depicted in Fig. 1.

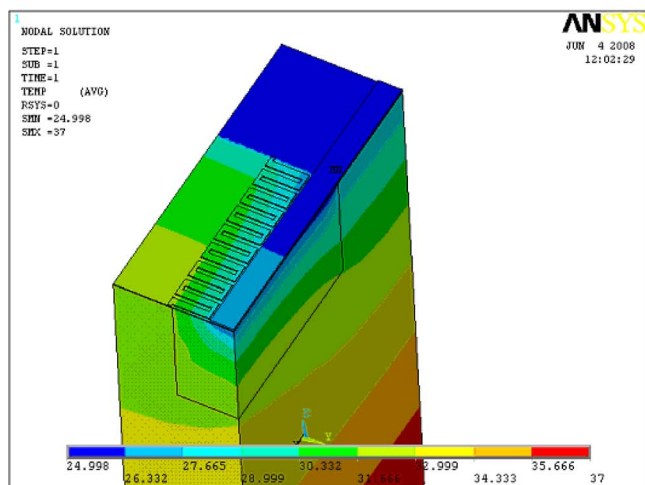
By using ANSYS software, we deploy finite element analysis (FEA) approach to simulate the temperature distribution. Figures 2(a)–2(c) display the temperature contour plots for thermoelectric structure on Si substrate in air ambient, a thermoelectric suspended membrane surrounded by ambient air, and a thermoelectric suspended membrane encompassed by vacuum cavities, respectively. There are 64 thermocouples on the suspended thermoelectric structure area. Due to this symmetric

structure, we only built one quarter of structure in the FEA model, as shown in Figs. 2(a)–2(c), while we did not create the cap structure in these FEA models and we assumed

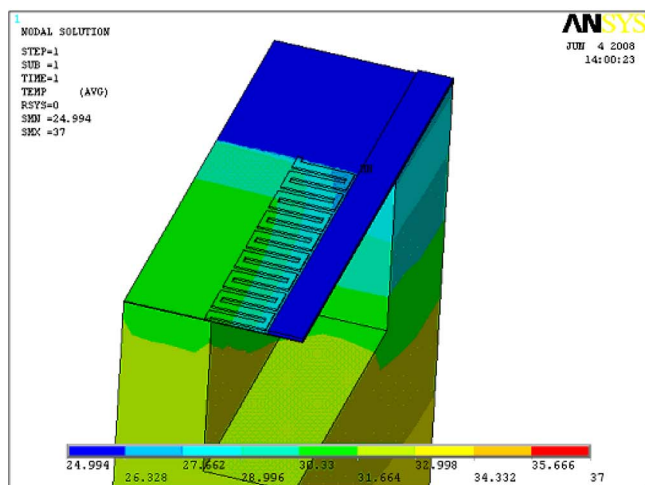
the top surface of device is either in air or in vacuum. The width, length, and thickness of a thermocouple strip are 6, 30, and  $1\ \mu\text{m}$ , respectively. In current study, we also introduce a new concept of HDP for enlarging the temperature difference between the cold and hot junctions as shown in Figs. 1 and 2(c). This HDP made of Al metal film in  $30\ \mu\text{m}$  width and of  $2\ \mu\text{m}$  thickness is arranged along the cold junctions of thermocouples. It should be noticed that only  $15\ \mu\text{m}$  wide HDP has been made in the quarter structure in FEA models. This simple and unique structure can effectively transfer the heat from cold junctions of thermocouples to the peripheral substrate surface where it is exposed in ambient air [Fig. 2(c)]. Without having this HDP, the heat from hot junction will be accumulated at the cold junction, since such heat cannot be dissipated via air and underneath silicon substrate in present device configuration. Thus the temperature difference between two junctions is expected to be very low, e.g., less than  $1^\circ\text{C}$ , for devices without HDP. In other



(a)



(b)



(c)

FIG. 2. (Color online) Temperature contour plots of MEMS TPG; (a) the TPG on Si substrate without underneath vacuum cavity and its surface exposed to air; (b) the TPG on Si substrate with underneath air-filled cavity and its surface exposed to air; (c) the TPG packaged in vacuum same as the configuration shown in Fig. 1, where the ambient air is maintained as 25 °C, the bottom surface of bottom Si substrate is kept as 37 °C, and the depth of vacuum cavity is 100  $\mu\text{m}$ .

words, the vacuum degree inside the wafer bonding packaged cavities needs to be high enough such that the heat path will be confined as the thermocouples membrane and HDP only. By measuring the heat loss from a hot object to the ambient as a function of gas pressure, MEMS based Pirani sensors can measure vacuum degree ranging from  $10^{-4}$  to 100 torr.<sup>11</sup> Second, a solder based wafer-bonded package for microbolometer array has been reported to show packaged vacuum of 1 mTorr.<sup>12</sup> Thus we suggest the vacuum degree in present design is about 1 mTorr because 1 mTorr is an achievable vacuum by wafer bonding and is gas pressure that the heat loss is dominant by the solid conduction, i.e., via thermoelectric membrane and HDP.

Figure 2(a) shows that the temperature difference between hot and cold junctions is very small for the thermoelectric structure without underneath air cavity. When an air cavity is created underneath the suspended thermoelectric structure, as shown in Fig. 2(b), the heat flux path is changed and the increased temperature difference is observed as well. However, significant heat conduction and convection still happen in the heat flux path from the suspended thermoelectric structure to ambient air. As further improvement, Fig. 2(c) shows the suspended thermoelectric structure of wafer-bonded vacuum package. This new vacuum packaged TPG can effectively increase the temperature difference through elimination of heat conduction and convection in air cavity.

In order to identify the temperature distribution of different thermocouple strips among the 16 strips, as shown in Fig. 2(c), we define each strip as the thermal leg from position 1 (the closest one to the edge of membrane next to the peripheral substrate) to position 16 (the one at the center of membrane). We extract the temperature at hot and cold junctions of said 16 strips and plot it in Fig. 3(a). The temperature difference reaches 6.3 °C at thermal leg 6 and gradually drops to 6.1 °C at leg 16 around center [Fig. 3(a)]. In contrast to the results shown in Figs. 2(c) and 3(a), almost no temperature difference and average temperature difference of 3–4 °C are observed in Figs. 2(a) and 2(b), respectively. Second we derived the temperature difference for 16 positions of thermal legs depending on various depths of underneath vacuum cavity of 100, 70, 50, and 20  $\mu\text{m}$ , respectively, as shown in Fig. 3(b). The maximum temperature difference is decreased down to 5.9, 5.6, and 5.25 °C for cases with vacuum cavities of 70, 50, and 20  $\mu\text{m}$ , respectively. Thus we maintain the vacuum depth of 100  $\mu\text{m}$  in all analytical simulation in the next section since it shows the highest temperature difference between hot and cold junctions along the 16 positions.

### III. ANALYTICAL MODELING OF TPG OUTPUT POWER

In the second part of simulation, we conduct the TPG output power optimization with respect to various widths of heat dissipation path in order to clarify the influence of heat dissipation path to the output power. First of all, we review the background physics. Equation (1) shows that the open circuit voltage  $U_o$  generated by a TPG is proportional to the

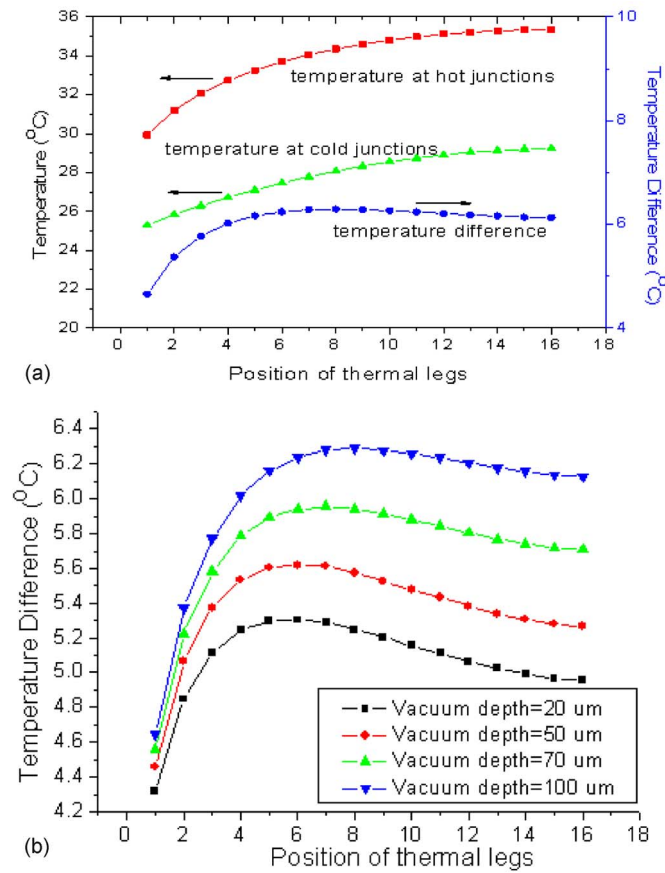


FIG. 3. (Color online) (a) Temperature distribution and the corresponding temperature difference vs the various position of thermal legs for the MEMS TPG device, in the case of the vacuum depth of 100 μm. (b) Temperature difference vs the various position of thermal legs in case of different depths of vacuum cavity.

number of thermocouples  $m$ , the relative Seebeck coefficient  $\alpha$  of the used thermocouple materials, and the temperature difference  $\Delta T_G$  between cold and hot junctions. We use 160 μV/K (Ref. 3) as the average Seebeck coefficient in the analytical simulation,

$$U_o = m\alpha\Delta T_G. \tag{1}$$

The maximum output power  $P_o$  can be achieved under matched load condition, i.e., the load resistance connected to the generator  $R_L$  equals the internal electrical resistance of the generator  $R_G$ ,

$$P_o = UI = \frac{U_o^2}{4R_G} = \frac{m^2\alpha^2}{4R_G}\Delta T_G^2, \tag{2}$$

where  $U$  is the output voltage under load and  $I$  is the electrical current. Assuming that the generator is connected to a cold reservoir and a hot reservoir via the thermal contact resistances  $K_C$  and  $K_H$ , respectively, the temperature drop across the generator  $\Delta T_G$  is expressed as Eq. (3), where  $K_G$  is the generators internal thermal resistance and  $\Delta T$  is the temperature difference between hot and cold reservoirs,

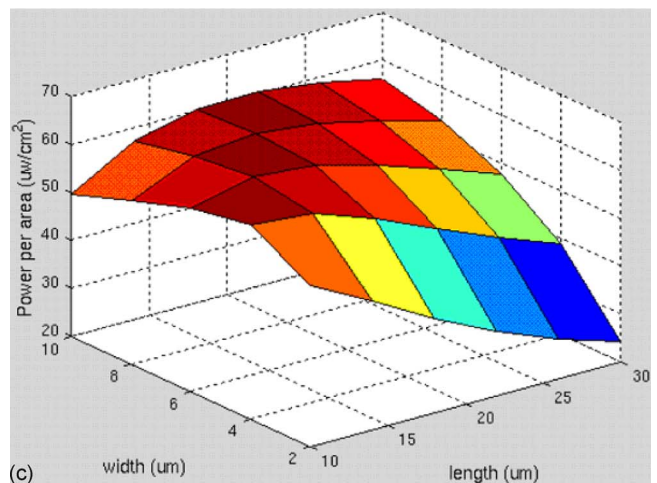
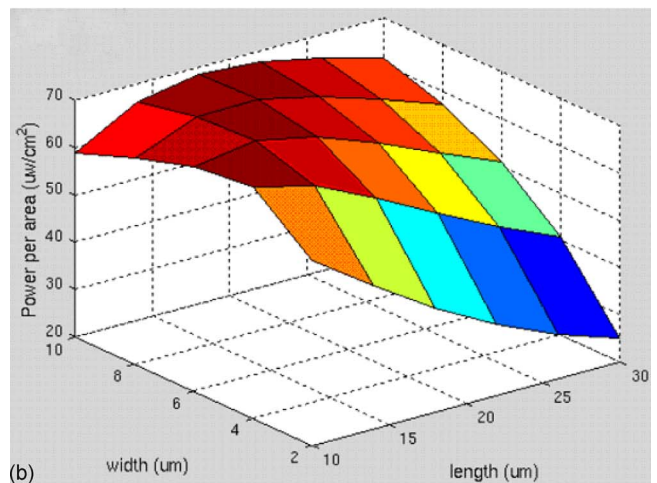
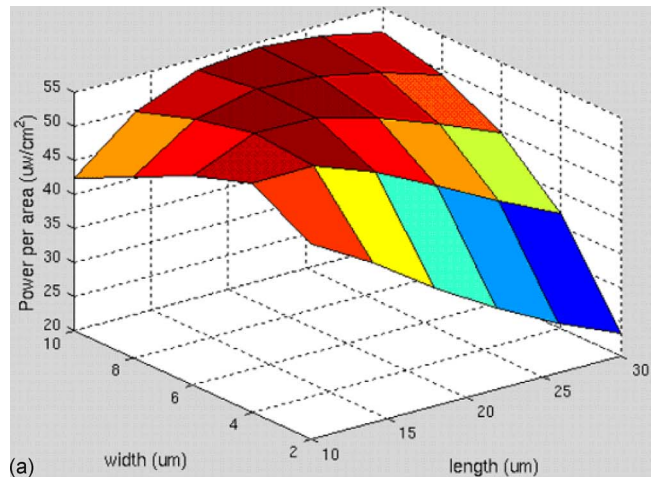


FIG. 4. (Color online) Optimized output power of TPGs with respect to various cases of different HDP widths: (a) HDP of 10 μm, (b) HDP of 20 μm, and (c) HDP of 30 μm.

$$\Delta T_G = \frac{K_G}{K_G + K_C + K_H}\Delta T. \tag{3}$$

For single thermal leg, the thermal resistance  $k$  and electrical resistance  $R$  are derived as Eqs. (4) and (5), where the  $\lambda$  is

TABLE I. Optimization of HDP with different widths.

Optimized items	Width of HDP ( $\mu\text{m}$ )		
	10	20	30
Output power per area of device ( $\mu\text{W}/\text{cm}^2$ )	54.2	68.6	60.5
Output power per area of thermocouples ( $\mu\text{W}/\text{cm}^2$ )	246.7	309.3	206.4
Length of thermal leg ( $\mu\text{m}$ )	22	18	20
Width of thermal leg ( $\mu\text{m}$ )	10	10	8

thermal conductivity and  $\rho$  is electrical resistivity, respectively,

$$k = \frac{l}{\lambda wt}, \quad (4)$$

$$R = \rho \frac{l}{wt}. \quad (5)$$

According to the approach discussed in Sec. II, we can derive the  $\Delta T$  for various cases in terms of different thermal leg widths and lengths, and width of HDP. Figures 4(a)–4(c) show the derived results in the three cases of HDP widths of 10, 20, and 30  $\mu\text{m}$ , respectively. The derived maximum output powers in these three cases are summarized in Table I. Since the effect of width and length of thermal leg on thermal resistance and electrical resistance are contradictory, thus there is an optimized combination of width and length in each case of different HDPs. The area of device is defined as the overall area including thermocouples, HDP, and peripheral substrate area. The observed maximum output power per area of device is 68.6  $\mu\text{W}/\text{cm}^2$  in the case of HDP of 20  $\mu\text{m}$ . On the other hand, we provide another index that is output power per area of thermocouples, when we exclude the area occupied by HDP. Interestingly device of HDP of 20  $\mu\text{m}$  still shows the highest output power as of 309.3  $\mu\text{W}/\text{cm}^2$ . Besides, device with HDP of 10  $\mu\text{m}$  shows the second highest output power as of 246.7  $\mu\text{W}/\text{cm}^2$  than

the output power of device with HDP of 30  $\mu\text{m}$ .

## IV. CONCLUSION

We investigated a new concept of CMOS MEMS based thermoelectric power generators with wafer-bonded vacuum cavities on both sides of suspended thermoelectric membrane. The calculated output power per area of device is 68.6  $\mu\text{W}/\text{cm}^2$  at initial temperature difference of 12  $^\circ\text{C}$  in which the induced temperature difference between two ends of thermocouple junctions is derived as 6.1  $^\circ\text{C}$ . This new concept is concluded as an effective approach to enhance the output power.

## ACKNOWLEDGMENTS

The authors acknowledge A\*STAR HOME 2015 National Research Programme (SERC Grant No. 0621150043) for the funding of this project and in-kind contribution from Institute of Microelectronics, A\*STAR. Chengkuo Lee would like to thank the support from the Faculty Research Fund under Grant No. R-263-000-358-112/133 for relative activities at the National University of Singapore.

- <sup>1</sup>S. Roundy, P. K. Wright, and J. Rabaey, *Comput. Commun.* **26**, 1131 (2003).
- <sup>2</sup>P. D. Mitcheson, E. M. Yeatman, G. K. Rao, A. S. Holmes, and T. C. Green, *Proc. IEEE* **96**, 1457 (2008).
- <sup>3</sup>T. VonBuren, T. P. D. Mitcheson, T. C. Green, E. M. Yeatman, A. S. Holmes, and G. Troster, *IEEE Sens. J.* **6**, 28 (2006).
- <sup>4</sup>M. Strasser, R. Aigner, M. Franosch, and G. Wachutka, *Sens. Actuators, A* **97–98**, 535 (2002).
- <sup>5</sup>A. Graf, M. Arndt, M. Sauer, and G. Gerlach, *Meas. Sci. Technol.* **18**, R59 (2007).
- <sup>6</sup>C.-H. Du and C. Lee, *Jpn. J. Appl. Phys., Part 1* **41**, 4340 (2002).
- <sup>7</sup>T. Huesgen, P. Woias, and N. Kockmann, *Sens. Actuators, A* **145–146**, 423 (2008).
- <sup>8</sup>Y. C. Lee, B. A. Parviz, J. A. Chiou, and S. Chen, *IEEE Trans. Adv. Packag.* **26**, 217 (2003).
- <sup>9</sup>M. Esashi, *J. Micromech. Microeng.* **18**, 073001 (2008).
- <sup>10</sup>C. Lee, *J. Jpn. Inst. Electron. Packaging* **10**, 42 (2007).
- <sup>11</sup>B. H. Stark and K. Najafi, *IEEE J. Microelectromech. Syst.* **13**, 147 (2004).
- <sup>12</sup>R. Gooch and T. Schimert, *MRS Bull.* **28**, 55 (2003).