AKASH KUMAR

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CAREER OBJECTIVE

I aspire to improve the lives of the many people that are living on this planet - be it by providing them with the world's best education or developing devices that can help improve the quality of lives. With my research in embedded systems, I hope to develop systems that can on one hand, benefit the aged and underprivileged people and on the other, provide an enriching experience for the masses. With my teaching, I aspire to train students to become leaders with high ethics and moral values, and the ability to design systems of the future.

EDUCATION

May 2005 – Apr 2009 Eindhoven University of Technology (TUe) & National University of Singapore

- **PhD** thesis title: "Analysis, Management and Design of Multimedia Multiprocessor Systems"**.**
- Published over 20 papers in leading system design conferences/ journals.
- Worked in close collaboration with many companies: **Silicon Hive, NXP Semiconductors, Philips**.
- Attended HiPEAC summer school on **Advanced Comp. Arch. and Compilation for Embedded Systems** in 2006.
- Attended ASCI spring school on **Embedded Systems** in 2006.

Jan 2003 – Dec 2004 National University of Singapore & Eindhoven University of Technology (TUe)

- **Master** of Technological Design (Embedded Systems). **GPA: 4.70/5.00.**
- Masters thesis title: "High-Throughput Reed Solomon Decoder for Ultra Wide Band."
- Received **Certificate of Merit** for the research done during internship at Philips Research Labs.

Jul 1999 – Dec 2002 National University of Singapore

- Accelerated **B. Eng**. (Computer Engineering) Program, **First Class Honours, GPA: 4.75/5.00.**
- Class **Valedictorian** (chosen out of about 800 students) and **Dean's List** on **4** occasions.

WORK EXPERIENCE

Jul 2009 – present Assistant Professor – National University of Singapore, Singapore

- Joined in Jul 2009 as a Visiting Fellow. Working as Assistant Professor since Jun 2011.
- Teaching courses offered by the Electrical and Computer Engineering (ECE) department.
- Pursuing research in the area of embedded multi-processor systems.
- Supervising students from undergraduate to post-graduate for research.

Jul 2011 – present Xilinx Trainer – Active Media Singapore

- Provide training on Xilinx FPGA architecture and design methodology.
- Specialized in Embedded Systems design (designed systems with up to 100 processors).
- Authorized to train on Zynq, Embedded Systems, Advanced features and techniques of Embedded Systems development, FPGA design, Advanced FPGA design, designing for performance, etc. courses.

May 2005 – Jun 2009 Research Assistant – Eindhoven University of Technology (TUe), The Netherlands

- Conduct research on embedded multiprocessor systems in order to make them predictable.
- Education: design and evaluate lab exercises for under-graduate and post-graduate courses.

Jan 2004 – Dec 2004 Research Intern – Philips Research Laboratories, The Netherlands

- Developed a high throughput, ultra low power Reed-Solomon decoder for Ultra Wide Band.
- **2 International Patents** filed over the work done during this stay, and **3 international publications**.

Jan 1999 – Dec 2003 Boarding Tutor, Raffles Institution Boarding School, Singapore

- Manage, supervise, motivate and teach a block of 90 students.
- Handle contingencies and organize activities for personality development of boarders.

Jun 2002 – Dec 2002 Intern – Merrill Lynch, Singapore

- Developed various automated applications using Java and Visual Basic for Applications.
- Conduct trainings for ML employees in database management system.

Jun 2001 – Aug 2001 Research Fellowship, California Institute of Technology, US

- 1 of the **3 students selected** from the entire National University of Singapore for this fellowship.
- Developed and implemented a scan-matching algorithm for sensor based motion planning.

RESEARCH AND TEACHING GRANTS

- Fault-tolerant Multi-processor Systems, DSO National Laboratories
  Principle Investigator, S$429,600, 06/2012-05/2015.
- Partially Reconfigurable Heterogeneous Multi-processor System-on-Chip, Singapore MoE ARC Grant
  Principle Investigator, S$179,990, 08/2011-07/2014.
- A Power-Efficient Heterogeneous Architecture and Run-Time Manager for Data Center Servers, A*Star Grant
  Co-Investigator, S$876,813, 08/2011-07/2014.
- Secured Large Scale Shared Storage System, A*Star Grant
  Collaborator, S$709,092, 08/2011-07/2014.
- Web-based toolkit for enhanced learning experience in digital fundamentals courses, NUS CDTL
  Principle Investigator, S$19,200, 08/2010-07/2012.
- Investigating feasibility of using fast reconfigurable logic in a typical MPSoC
  Principle Investigator, € 5,000 (equivalent to S$ 10,000), 01/2007-04/2007.
- A run-time admission controller for multiple applications on FPGA
  Principle Investigator, € 5,000 (equivalent to S$ 10,000), 09/2007-12/2007.

TEACHING

Following are the courses that I have (co-)taught during my appointment at NUS and TUe. I have had an opportunity to teach classes of varying sizes – from 400 students to only 12 students in a class. In all my courses I ensure that students need to work on design problems in small groups to understand the concepts better.

E4214 Real-Time Embedded Systems (Aug 2009, Aug 2010, Aug 2011, Aug 2012)

- This course covers topics in real-time embedded systems like task scheduling, shared resources, real-time operating systems, concurrent programming and deadlock management.
- 35% of the grade is determined by a project where students have to design a real-time system running on a dual-Microblaze based platform on a Xilinx FPGA. The project last semester was to develop a controller for 5-a-side soccer, compete against other teams and display the progress of the game on a VGA port connected to the FPGA board.
- Obtained Xilinx sponsorship for the top three team prizes and software license for 100 students.
- Attended by about 80 students; **nominated for Best Teacher Award** by the students.

EE4218 Embedded Hardware System Design (Jan 2010, Jan 2011, Jan 2012, Jan 2013)

- This course covers topics in embedded hardware design like system specification and modelling, behavioural synthesis, logic synthesis and physical synthesis.
- 60% of the grade is determined by a series of projects which involve designing an embedded system on a Xilinx FPGA in VHDL. The project in the ongoing semester is to implement 128-bit Advanced Encryption Standard (AES) decryption algorithm in software and hardware and compare.
- Attended by about 95 students; **nominated for Best Teacher Award** by the students.

EE2006 Digital Design/EE2020 Digital Fundamentals (Jan 2010, Aug 2010, Jan 2011, Aug 2011, Jan 2013)

- This course is an introductory level course in digital circuits for second-year students. The course starts with a revision of Boolean algebra and number systems, explains various MSI combinational and sequential circuit elements, and introduces VHDL and algorithmic state machines.
- 40% of the grade is determined by a digital design project and a VHDL programming assignment.
- Attended by about 500 students annually; **nominated for Best Teacher Award** by the students.

5KK53 Implementing Large Scale Embedded Processors on Deep-Submicron Silicon (Apr 2006)

- This is a course for Masters Students in embedded processor design at Eindhoven University of Technology (TUe). The students have to partition and map a JPEG decoder on an MPSoC platform.
- Course organized in collaboration with Silicon Hive and Philips Research (now NXP Semiconductors)
- 100% of the grade is determined by the project; carried out on the multiprocessor system developed by me.
- Attended by about 50 students.

PATENTS

- **Method and Apparatus for Syndrome Calculation**
  International Application Number: PCT/IB2006/052151, filed on June 28, 2006.
  Europe Patent Application Number: 05105878.2, filed on June 30, 2005.
- **Pipelined Reed-Solomon Decoder**
  International Application Number: PCT/IB2006/054745, filed on Dec 11, 2006.
  Europe Patent Application Number: 05111971.7, filed on Dec 12, 2005.

HONOURS AND AWARDS

- **Singapore Mathematical Olympiad Gold** medalist.
- **1st place** in **IEEE – NTU Mathematics Olympiad**.
- Awarded **National Talent Search Scholarship** by **Human Resource Development Ministry, India.**
- Recipient of **SIA Scholarship** for Pre-University and Bachelors study in **RJC** and **NUS**.
- Awarded **DTI scholarship** (managed by EDB) for **Masters in Embedded Systems** in NUS.
- **Runner-up** in the first International **IEEE Extreme** Online Programming contest, 2006.
- **On-stage finalists** in first International **Tata Crucible** in NUS – "India's toughest **business** Quiz", 2007.
- **10th place** in annual **ACM** International Collegiate Programming Contest regional contest (ICPC).

RESEARCH OVERVIEW

The focus of my research is to design predictable multi-processor systems – predictable in terms of both the architecture and the applications. Multiprocessor systems-on-chip (MPSoCs) have been proposed as a solution to rising power and area of modern embedded systems. These systems are becoming increasingly heterogeneous with use of dedicated IP blocks and application domain specific processors. To achieve high performance in such systems, the limited computational resources must be shared. The concurrent execution of dynamic applications on shared resources is a potential source of interference. Modelling and analyzing this interference is a key to building cost-effective systems which can deliver the desired performance of the applications. However, the following four main issues remain that have been the focus of my research over the last six years.

- Design such platforms from a high-level description automatically such that they consume less time and are not prone to error; contrary to existing manual techniques.
- Program these heterogeneous multiprocessor platforms such that the functional requirement is met.
- Design a run-time resource manager analogous to an operating system for such heterogeneous MPSoCs.
- Analyze the behaviour of multiple applications that share resources and thereby suffer from resource contention.

Some key achievements during this research are listed below:

- A detailed analysis of the problems encountered when mapping multiple applications on an MPSoC platform was carried out, and measures provided to overcome these problems. The findings and solutions are published in **DSD 2006**, and later in **Journal of System Architecture 2007.**
- A resource manager was developed for admission control and budget enforcement to ensure all applications can meet their performance requirements even when sharing platforms with other concurrent applications. The results are published in **ESTIMEDIA 2006.** The work is now being implemented on FPGA.
- The first ever working prototype of Silicon Hive VLIW cores integrated with Æthereal network-on-chip (developed by Philips Research) on an FPGA was created. This integrated multiprocessor platform is now used for a **Masters course** at TUe. The results are published in **DATE 2007**.
- A probabilistic technique was developed to model resource contention when multiple applications are executing simultaneously on a multi-processor platform. The results are published in proceedings of **DAC 2007**. The technique was later refined and published in **TCAD 2010**.
- A flow to generate an MPSoC platform was designed – both hardware and software, directly from a very high-level (SDF) description of multiple applications. This is first design-flow that allows such automated synthesis. This flow **MAMPS** was **released in 2007 (http://www.es.ele.tue.nl/mamps),** and the details are described in proceedings of **FPL 2007,** and in **ToDAES 2008** with support for multiple use-cases. **MAMPS** is now being used by 12 research groups. Various enhancements have been done by many students since.

STUDENT SUPERVISION

PhD Students

- **Pham Nam Khanh (2012-contd):** Mapping and scheduling for partially reconfigurable platforms.
- **Li Ang (2012-contd):** Code optimization with cache consideration.
- **Hoo Chin Hau (2012-contd):** 3D FPGA architecture.
- **Anup Kumar Das (2011-contd):** Fault-tolerance design and scheduling for multi-processor platforms.
- **Ahsan Shabbir (2007-2011):** Resource mapping and management for predictable multi-processor platforms.
- **Amit Kumar Singh (2009-2012):** Run-time mapping of communicating tasks on multi-processor platforms.

Masters Students

- **Sun Longkai (2012-contd):** Mapping and design for partially reconfigurable heterogeneous multi-processor platforms.
- **Ang Zhi Ping (2012-contd):** Low-power and low-cost image encoding and decoding for unmanned aerial vehicles.
- **Sreejaya Viswanathan (2011):** Hardware/ Software co-design of image processing application for human gesture recognition on FPGA.
- **Raajesh Kotteeswaran (2011):** Hardware/software co-design of H264 decoder on FPGA.
- **Sheng Wang (2010):** Power optimization for SDM-based NoC by load balancing and frequency scaling.
- **Manmohan Manoharan (2010):** Developing dataflow analysis techniques for a spatial-division-multiplexing based network-on-chip.
- **Michiel Rooijakkers (2009):** Web-server controlled multi-tasking on an FPGA-based multi-processor system.
- **Thom Gielen (2007-2008):** Deriving a parallel description of an application from its sequential description, and integrating it in the **MAMPS** flow**.**
- **Alberto (2008):** Developing a communication assist for MPSoC platforms.
- **Mark Sleegers (2006):** Developed an audio-conferencing program to run using Ethernet on FPGA.

Bachelors Students

- **Hoo Chin Hau (FYP 2011-2012):** Designing an area-efficient partially reconfigurable crossbar switch with low-reconfiguration delay.
- **Pranay Puranik (FYP 2011-2012):** Implementing financial algorithm of distance to default on FPGA, with a focus on log-likelihood function.
- **Lo Yat Piu (FYP 2011-2012):** Implementing financial algorithm of distance to default on FPGA, with a focus on implied asset value.
- **Izaan Mohammed (FYP 2011-2012):** Implementing financial algorithm of distance to default on FPGA, with a focus on overall flow and fmincon solver.
- **Kanav Khurana (FYP 2011-2012):** Brain computer interfacing on FPGA platforms.
- **Pooja Gupta (FYP 2011-2012):** Brain computer interfacing on FPGA platforms.
- **Celine Leow (FYP 2011-2012):** Error-correcting codes for fault-tolerant network-on-chip platforms.
- **Anu Ramanathan (FYP 2011-2012):** Making networks-on-chip fault-tolerant with redundant serializers.
- **Li Jiashu (FYP 2011-2012):** A Design Flow for Partially Reconfigurable Heterogeneous MPSoCs.
- **Tian Yao (FYP 2011-2012):** CMOS Wide-Band LO design for Bio-Medical Application.
- **Yap Tshun Hau (FYP 2011):** Designing a fault-tolerant network interface receiver.
- **Varun Sivamani (FYP 2011):** Visual content extraction system.
- **Aayush Sharma (FYP 2011):** Configuring iTwin for Mac environment.
- **Vaibhav Kothari (FYP 2011):** Remote desktop connection with 256-bit encryption for iTwin.
- **Li Jiashu (UROP 2011):** Transferring video via Ethernet to an FPGA board.
- **Chew Chong Ching (FYP 2010-2011):** Developing a fault-tolerant network interface for Spatial Division Multiplexing based networks.
- **Lim Boon Hwee Matthew (FYP 2010-2011):** Runtime Reconfiguration Overhead Reduction During Use Case Switching in Spatial Division Multiplexing Network-on-Chip.
- **Yong Ho Yuet (FYP 2010-2011):** Task Scheduling for Fault Tolerance on Network-based Multiprocessor System
- **Joseph Yang (FYP 2009-2010):** Developing a spatial division multiplexing based network-on-chip with static guarantees.
- **Abhinav Krishna (FYP 2007-2008):** Work on extending **MAMPS** with mapping information.
- **Priyantha De Silva(FYP 2007-2008):** Map MPEG-4 decoder on multi-processor FPGA platform.

Theses and Oral Examination Committees

- I participated in theses and/or oral examination committee of the following students: Panikkaveettil Shamsudheen Shija, Syed Rizwan, Hong Zhiqian, Wang Tao, Waqas Muhammad, Loke Mei Hwan, Hoong Maeng Chan, Zhu Cenzhe, Yu Heng, S.P.T. Krishnan, Hong ZhiQian, Subash Kuselan, Zhang Wenjuan.

CONFERENCES AND JOURNAL REVIEW

- **Reviewed papers for the following conferences/journals in the years mentioned below.**
  - **ACSD** (Analysis of Concurrency in System Design): 2008
  - **CASES** (Compilers, Architecture, and Synthesis for Embedded Systems): 2011, 2013
  - **DAC** (Design Automation Conference): 2009, 2010, 2011, 2012, 2013
  - **DATE** (Design Automation and Test in Europe): 2007, 2008, 2009, 2011
  - **Estimedia** (Embedded Systems for Real-Time Multimedia): 2006 and 2007
  - **ETRI Journal** (Electronics and Telecommunications Research Institute): 2007, 2009, 2011
  - **IJCAT** (International Journal of Computer Applications and Technology): 2012
  - **ISCAS** (International Symposium on Circuits and Systems): 2009, 2010, 2011, 2012
  - **ISLPED** (International Symposium on Low Power Electronic Design): 2012
  - **IEEE Embedded System Letters:** 2010
  - **IEEE Transactions Education:** 2013
  - **IEEE Transactions on Circuits and Systems II**: 2012
  - **JCSC** (Journal or Circuits Systems and Computers): 2012
  - **ACM TECS Journal** (Transactions on Embedded Computing Systems): 2011, 2012, 2013
- **Technical Program Committee member for**
  - **SCOPES** (Software and Compilers for Embedded Systems): 2011, 2012, 2013
  - **ICON** (International Conference on Networks): 2011, 2012
  - **FPL** (Field Programmable Logic and Applications): 2013
  - **FPT** (Field Programmable Technologies): 2013
  - **CASES** (Compilers, Architecture and Synthesis for Embedded Systems): 2013

BACHELORS/MASTERS PROJECTS

Jan 2004 – Dec 2004 **Philips Research Laboratories**, Eindhoven

- Design and develop high-throughput and low power Reed Solomon Decoder for Ultra Wide Band.
- The decoder was written in VHDL, and optimised for both ASIC and FPGA implementations.
- New ideas proposed and implemented to achieve high throughput needed for UWB communication.
- **2 International Patents** filed over the novel high throughput and low power RS decoder design.
- The results of the designs were further published in **3 international publications.**

Platform and Languages: Linux, C, VHDL
Packages used: Precision RTL, Altera Quartus II, Ambit, Cadence SimVision, Diesel, Synplicity

Jan 2003 – Dec 2003 **Masters Research Project**

- The objective of the project was to develop a system that could track the movements of a wireless pen and re-draw them on a computer screen in real-time.
- The system consisted of a wireless pen that was fit with an ultrasound (US) transmitter, receiver system consisting of four US receivers, a TI DSP, and a USB interface to the PC.
- The precise position of the pen was computed using Time Delay Estimation.
- I was responsible for programming the DSP, the DSP-USB interface and part of the application, apart from developing the overall design concept and the algorithm used for position estimation.
- The project also provided with valuable experience of working in a multicultural team.

Platform and Languages: TI DSK6711, THS1206, TUSB3210, PIC12F675, C, ASM, Matlab, C++.
Packages used: Code Composer Studio, Visual Studio, MPLAB IDE.

Other Hardware Projects

- **16-bit barrel shifter:** Designed and did the layout using the Cadence Virtuoso layout editor.

- **Audio amplifier project:** Worked in a team of 3, and I was responsible for the pre-amplifier. Designed and fabricated a PCB for a stereo system and also implemented the 5-band equaliser on it. The simulations were done in E-workbench and PCB boards were designed using Protel.
- **Talking multi-meter:** Designed and implemented using Intel 80188 µP. An LCD screen was also incorporated.
- **Board Game:** Designed using Cypress CPLD and programmed using VHDL.

Other Software Projects

- **Final Year Project:** Developed a new algorithm for scheduling bursts in Wavelength Division Multiplexing Optical Burst Switched networks. Results published in an IASTED WOC Conference.
- **Bluetooth simulation model with SHESim:** Worked in a team of 7 people; I was in charge of the application and Service Discovery Protocol layer.
- **ASM simulator and debugger:** Developed in C++ as part of a computer architecture course.
- **Video broadcast application:** Written using Java Media Framework for use in an Ethernet network.
- **Travel Guidance System:** a GUI-based program in Java for displaying maps/routes based on input.
- **UDP based File Transfer Protocol (FTP):** for secure file transfer in real time, implemented in C.
- **Airline reservation system:** Developed using client-server protocol in C. The reservation system also communicated with the bank server to process transactions.

TECHNICAL SKILLS

- **Hardware:** Texas Instruments DSK (DSP Starter Kit) 6711; worked extensively on a number of Xilinx FPGA boards - Celoxica, Nallatech and Digilent boards; Altera FPGA boards.
- **Hardware Design Packages:** Xilinx ISE, EDK and Chipscope, Synplify Pro, Altera Quartus, Celoxica DK Design Studio, TI Code Composer Studio, Cadence Virtuoso, Cadence SimVision, Ambit, Protel.
- **Languages:** VHDL, C, C++, Java, Matlab, Handel-C, ASM, Visual Basic, HTML, SQL, uC-OS/II (RTOS).

LANGUAGE SKILLS

- **English:** Fluent in reading, writing and conversing.
- **Hindi:** Fluent in reading, writing and conversing.
- **Dutch:** Fluent in reading, writing and conversing.

OTHER ACTIVITIES

- **Gliding** for 4 years in Eindhoven University student flying club. Certified **solo glider pilot**.
- Committee member of **Indian Instrumental Ensemble (IIE)** at university and a senior **violin** player. Organised and participated in annual concerts on and off-campus.
- Learning **North-Indian classical music** (Hindustani); performed on a number of occasions.
- Have been learning various **latin and style-dances** since last 4 years.
- Play **badminton** and **squash** regularly.

REFEREES

- **Prof. Dr. Henk Corporaal:** PhD advisor at TU/e (2005-2009) and Masters Project (2003-2004).
  Email: h.corporaal@tue.nl. Tel: +31-40-247-5462/5195.
- **Prof. Dr. Sergei Sawitzki:** Supervisor at Philips Research. Currently Prof at Univ. of App. Sciences, Germany.
  Email: saw@fh-wedel.de. Tel: +49-4103-8048-37.
- **Dr. Bart Mesman:** PhD advisor at TU/e (2005-2009).
  Email: b.mesman@tue.nl. Tel: +31-40-247-3612/5195.
- **Dr. Yajun Ha:** PhD advisor at NUS (2005-2009).
  Email**:** elehy@nus.edu.sg. Tel: +65-6516-2258.
- **Ir. Jos Huisken:** Collaborator at Silicon Hive (2005-2006). Presently with IMEC-NL, Eindhoven
  Email: jos.huisken@imec-nl.nl. Tel: +31-40-277-4407.

List of Publications

Books, Journals and Book Chapters

1. **[TECS '13]** Energy-Aware Task Mapping and Scheduling for Reliable Embedded Computing Systems
   Anup Das, **Akash Kumar**, Bharadwaj Veeravalli
   In: ACM Transactions on Embedded Computing Systems. ACM, 2013.

2. **[BookChapter '13]** Implementing Time-Constrained Applications on a Predictable MPSoC
   Sander Stuijk, **Akash Kumar**, Roel Jordans and Henk Corporaal
   In M. Qadri and S Sangwine, editors, Multicore Technology: Architecture, Reconfiguration, and Modeling
   ISBN: 978-1-439880-63-0. CRC Press, Boca Raton, Fl, USA, 2013.

3. **[FGCS '13]** Communication and Migration Energy Aware Task Mapping for Reliable Multiprocessor Systems
   Anup Das, **Akash Kumar**, Bharadwaj Veeravalli
   In: Future Generations Computing Systems. 2013,
   Elsevier, 2013.

4. **[FCS '13]** CADSE: communication aware design space exploration for efficient run-time MPSoC management
   Amit Kumar Singh, **Akash Kumar**, Jigang Wu, Thambipillai Srikanthan
   In: Frontiers of Computer Science. 2013, ISSN: 2095-2228.
   Springer, 2013.

5. **[TE '13]** Project-based Learning in Embedded Systems Education Using FPGA Platform
   Akash Kumar, Shakith Fernando and Rajesh C Panicker
   Accepted in: IEEE Transactions on Education. 2013, ISSN: 0018-9359. IEEE, 2013.

6. **[ToDAES '12]** Accelerating Throughput-aware Run-time Mapping for Heterogeneous MPSoCs
   Amit Kumar Singh, **Akash Kumar** and Thambipillai Srikanthan
   In: ACM Transactions on Design Automation of Electronic Systems. Vol 18, Issue 1, Dec 2012, pp. 1-29,
   ISSN:1084-4309. ACM, 2012.

7. **[Book '10]** Multimedia Multiprocessor Systems: Analysis, Design and Management
   Akash Kumar, Henk Corporaal, Bart Mesman, Yajun Ha.
   1st Edition., 2010, XVI, 163 pages, Hardcover.
   ISBN: 978-94-007-0082-6. Springer, 2010.

8. **[JSA '10]** *Communication-aware Heuristics for Run-time Task Mapping on NoC-based MPSoC Platforms*
   Amit Kumar Singh, Thambipillai Srikanthan, **Akash Kumar**, Wu Jigang.
   In: *Journal of Systems Architecture.* Vol 56, Issue 7, July 2010, pp. 242-255,
   ISSN: 1383-7621. Elsevier, 2010.

9. **[JSA '10]** *CA-MPSoC: An Automated Design Flow for Predictable Multi-processor Architectures for Multiple Applications*
   Ahsan Shabbir, **Akash Kumar**, Sander Stuijk, Bart Mesman, Henk Corporaal
   In: *Journal of Systems Architecture.* Vol 56, Issue 7, July 2010, pp. 265-277,
   ISSN: 1383-7621. Elsevier, 2010.

10. **[TCAD '10]** *Iterative Probabilistic Performance Prediction for Multi-Application Multi-Processor Systems*
    Akash Kumar, Bart Mesman, Henk Corporaal, Yajun Ha.
    In: IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. Vol 29, Issue 4, April 2010, pp. 538-551, ISSN:0278-0070. IEEE, 2010.

11. **[CCIS '09]** *Enabling MPSoC Design Space Exploration on FPGAs*
    Ahsan Shabbir, **Akash Kumar**, Bart Mesman and Henk Corporaal.
    In: D.M.A. Hussain, A.Q.K. Rajput, B.S. Chowdhry and Q. Gee (Eds): Wireless Networks, Information Processing and Systems, Communications in Computer and Information Science Series.Vol. 20, pp. 412-421, ISBN: 978-3-540-89852-8. Springer, 2009.

12. **[ToDAES '08]** *Multi-processor Systems Synthesis for Multiple Use-Cases of Multiple Applications on FPGA*
    Akash Kumar, Shakith Fernando, Yajun Ha, Bart Mesman and Henk Corporaal.
    In: ACM Transactions on Design Automation in Electronic Systems. Vol 13, Issue 3, July 2008, pp. 1-27. ISSN: 1084-4309. ACM 2008.

13. **[JSA '08]** *Analyzing Composability of Applications on MPSoC Platforms*
Akash Kumar, Bart Mesman, Bart Theelen, Henk Corporaal and Yajun Ha
In: Journal of Systems Architecture. Vol 54, Issue 3-4, March-April 2008, pp. 369-383.
ISSN: 1383-7621. Elsevier B.V., 2008.

14. **[BookChapter '06]** *High-Throughput and Low-Power Reed Solomon Decoded for Ultra Wide Band*
Akash Kumar and Sergei Sawitzki
In: Wim Verhaegh, Emile Aarts, and Jan Korst(Eds.): Intelligent Algorithms, Philips Research Book Series, Vol. 7, pp. 299-316, ISBN: 1-4020-4953-6. Springer, 2006.

15. **[ComCom '05]** *Efficient techniques for improved QoS performance in WDM optical burst switched networks*
Gurusamy Mohan, **Akash Kumar** and Maskara Ashish
In: Computer Communications, Vol. 28, Issue 7, 2 May 2005, pp. 754-764. ISSN: 0140-3664.
Science Direct, 2005. doi:10.1016/j.comcom.2004.10.007

16. **[LNCS '03]** *Membrane systems and distributed computing*
G. Ciobanu, R. Desai, **Akash Kumar**
In: Gh.Paun, G.Rozenberg, A.Salomaa, C.Zandron (Eds.): Membrane Computing, Lecture Notes in Computer Science, Vol. 2597, pp. 187-202, ISSN: 0302-9743. Springer, 2003.

Conference Papers

1. **[FPT '13]** Real-time and Low Power Embedded L1-Optimization Solver Design
Zhi Ping Ang and **Akash Kumar**
In: Proceedings of the International Conference on Field-Programmable Technology, 8-10 December 2010, (FPT), 9-11 Dec 2013. Kyoto, Japan. IEEE.

2. **[DFT '13]** Run-time mapping for reliable many-cores based on energy/performance trade-offs
Cristiana Bolchini, Matteo Carminati, Antonio Miele, Anup Das, **Akash Kumar** and Bharadwaj Veeravalli.
In: Proceedings of the 16th IEEE Symp. Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), 2-4 Oct 2013
New York City, USA. IEEE.

3. **[CASES '13]** Aging-aware Hardware-Software Task Partitioning for Reliable Reconfigurable Multiprocessor Systems
Anup Das, Akash Kumar and Bharadwaj Veeravalli.
In: Proceedings of the International Conference on Compilers Architectures and Synthesis of Embedded Systems (CASES), Embedded Systems Week, 29 Sep-4 Oct 2013.
Montreal, 2013. ACM/IEEE.

4. **[DSD '13]** RAPIDITAS: RAPId Design-space-exploration Incorporating Trace-based Analysis and Simulation
Amit Kumar Singh, Anup Das and Akash Kumar
In: Proceedings of international conference on digital systems design (DSD), 4-6 Sep 2013
Santander, Spain. IEEE.

5. **[DSD '13]** Incorporating Energy and Throughput Awareness in Design Space Exploration and Run-time Mapping for Heterogeneous MPSoCs
Nam Khanh Pham, Amit Kumar Singh, Akash Kumar and Mi Mi Aung Khin
In: Proceedings of international conference on digital systems design (DSD), 4-6 Sep 2013
Santander, Spain. IEEE.

6. **[FPL '13]** Improving Autonomous Soft-error Tolerance of FPGA through LUT Configuration Bit Manipulation
Anup Das, Shyamsundar Venkataraman and Akash Kumar
In: Proceedings of the 23rd International Conference on Field Programmable Logic and Applications (FPL), 2-4 Sep 2013. Porto, Portugal. IEEE.

7. **[FPL '13]** A Directional Coarse-Grained Power Gated FPGA Switch Box and Power Gating Aware Routing Algorithm
Chin Hau Hoo, Yajun Ha and Akash Kumar
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