Assignment

1. Read the setup file and make yourself familiar with Linux environment. The pointers to relevant documentation are also given in this document.
2. Complete the cookbook on compiling core and answer the questions given there.
3. Complete the cookbook on compiling program and answer the questions given there.
4. Read the documentation on basic power estimation, and also in **$HIVEBIN/../doc/power_estimation_tutorial.pdf**.
5. Start with the application (**fdct_original.c**) available on the project website: http://www.es.ele.tue.nl/~akash/5kk73.php.
   a) This program can be compiled for a general processor. Make the modifications to make it run on both processors (*pearl* and *pearl_is3*) generated in Step 2. How many cycles does it take on each processor?
   b) Modify the processor pearl_is3 such that the parallelism in the given application can be exploited. *(Hint: perhaps add more register files and memories.)*
   c) Optimize the application code of **fdct_original.c** for your target processor. *(Hint: Refer to Chapter 8 of HiveSDK.pdf for tips.)*
   d) Check the cycle count and power consumption of your application on your processor.
   e) Iterate over steps (b), (c) and (d) to reduce the cycle count as much as possible.
6. When you are finished, make a file called *name.txt* in your home directory containing *your name* and *student number*.

Deliverables

A small report in the following format.

Name: _____
Student number: _____

Step 2: Compiling the core
Answer 1:
Answer 2:
Answer 3:
Answer 4:
Answer 5:

Step 3: Compiling the program
Answer 1:
Answer 2:
Answer 3:
Answer 4:

Step 4: Optimizing the given application
Answer (a): Cycles: *pearl*: _____ cycles, *pearl_is3*: _____ cycles.
Energy:*pearl*: _____ Joules, *pearl_is3*: _____ Joules.
Power: pearl: _____ Watts, *pearl_is3*: _____ Watts.

Answer (b-d):

- Explain the final processor architecture (include a screen-shot from *corebrowser*).
- Explain the optimizations made to the application.
- How good is your hardware utilization (check the html directory and report results)?
- Report energy, area and $T_{execution}$ of the architectures / mappings you have researched.

- You may add a Pareto curve of these architectures (either one 3-D plot, or several 2-D; in the latter case e..g. Time-Area, and Time-energy)
- Justify your architecture, and explain the trade-offs in processor-area, application cycle count, power and energy consumption.

Bonus

The student or group with the best design will get a bottle of wine.