Keynote speech on
"Designing (Relatively) Unreliable Systems with (Highly) Unreliable Components"

SPEAKER:

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Conference: IEEE NEWCAS 2016
Date: June 28, 2016
Venue: Vancouver (Canada)

In this keynote, Prof. Alioto shares his vision on the path towards sustainable and continuous reduction in energy consumption of integrated circuits in the next decade, in spite of the Moore's law slowing down. Adding the energy-quality scaling as a new design dimension promises large energy gains in applications that have become prominent with cloud and mobile computing, and even larger gains in IoT.

ABSTRACT: Ten years after the new breed of ideas on how to design reliable systems with unreliable components, the design challenges posed by variations are harder than ever. To reduce the large energy cost of computational correctness due to variations, the VLSI community is now exploring ways to embrace imperfect computation, instead of over-constraining circuits/systems to hide the natural imperfection of hardware. However, the field of "approximate computing" is still in its infancy, and most of the related work is highly fragmented and not really focused on the real challenges.

In this talk, a vision on how mainstream processing platforms can incorporate error-tolerant computation will be presented. In particular, we will introduce a unitary framework for systems that dynamically trade off energy and quality of computation, depending on the application and the user's requirements. Fresh concepts to preserve the economy of scale offered by todays' design approaches will be discussed, along with ways to incorporate dynamic energy-quality management in general-purpose systems, designed with existing EDA tools, and programmed with existing software programming models (or so). Variation-aware circuit techniques and design strategies will be discussed to enable dynamic and wide energy-quality adjustment in sub-32nm technologies, from error-tolerant to error-free. Appropriate abstractions, architectures and control schemes will be discussed to propagate such capability at all levels.

BIO: Massimo Alioto is Associate Professor at the Department of Electrical and Computer Engineering, National University of Singapore, where he leads the Green IC group and the Integrated Circuits and Embedded Systems area. Previously, he was Associate Professor at the University of Siena, Visiting Scientist at Intel Labs – CRL (2013), Visiting Professor at the University of Michigan - Ann Arbor (2011-2012), University of California – Berkeley (2009-2011) and EPFL - Lausanne.

He is (co)author of 220+ publications on journals (80, mostly IEEE Transactions) and conference proceedings, and two books with Springer. His primary research interests include ultra-low power VLSI circuits, self-powered and wireless nodes, near-threshold circuits for green computing, error-aware and widely energy-scalable VLSI circuits, circuit techniques for emerging technologies.

Prof. Alioto was the Chair of the "VLSI Systems and Applications" Technical Committee of the IEEE CAS Society (2010-2012), and Distinguished Lecturer (2009-2010). He is currently Associate Editor in Chief of the IEEE Transactions on VLSI Systems. He also serves or has served as Associate Editor of eight journals (e.g., ACM Transactions on Design Automation of Electronic Systems, IEEE Transactions on CAS - part I). He served as Guest Editor of various journal special issues (including the issue on "Ultra-Low Voltage Circuits and Systems for Green Computing" published on Dec. 2012 on IEEE Transactions on Circuits and Systems – part II). He was Technical Program Chair of the ICECS 2015, VARI 2015, ICECS 2013, NEWCAS 2012 and ICM 2010 conferences, and Track Chair in a number of conferences (ICCD, ISCAS, ICECS, VLSI-SoC, APCCAS, ICM). He is currently member of the IEEE CASS Board of Governors. Prof. Alioto is an IEEE Fellow.